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GSN Optical: How to solve the problem

Arie van Praag, CERN, 3 April 2000

Abstract

The Gigabyte System Network (GSN) standard specifies two media for connection: a Copper Cable connection, used up to now, and a Fibre Optics connection using a 12 channel flat cable. As no work had been done on the optical connection up to now, it was decided to start a project in this direction at CERN in collaboration with industry. It is explained why a different approach was taken to that foreseen as a GSN optical standard and how an optical connection that works at the full GSN bandwidth was realised. It is now decided that this technology will be the new GSN Optical standard.

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The Gigabyte System Network (GSN) standard specifies two media for connection: a Copper Cable connection, used up to now, and a Fibre Optics connection using a 12 channel flat cable. As no work had been done on the optical connection up to now, it was decided to start a project in this direction at CERN in collaboration with industry. It is explained why a different approach was taken to that foreseen as a GSN optical standard and how an optical connection that works at the full GSN bandwidth was realised. It is now decided that this technology will be the new GSN Optical standard.

A Short Introduction to GSN:

The **G**igabyte **S**ystem **N**etwork is a 10 Gigabit/s network standardised by ANSI NCITS and ISO/IEC under the project name HIPPI-6400 [1]. This high speed network was from the beginning developed for a very high transfer speed with a very low network latency. A maximum of functionality is executed in hardware. The transfer is done in small micropackets and the transfer medium is divided into four multiplexed Virtual Channels to avoid congestion by large data streams. Each of the Virtual Channels has its own end to end CRC error checking extended with an overall link CRC. A refined look-ahead mechanism avoids end point congestion [2]. All this interface functionality of the physical link is built into a single silicon chip called SUMAC. The use of this chip by all manufacturers of GSN equipment leads to a very high factor of compatibility. In order to keep transfer latency low GSN is accompanied with an operating system bypass protocol "ST" (Scheduled Transfer) that works also with IP and SCSI transfers [3][4]. The ST protocol is also successfully demonstrated for other network technologies such as Fibre Channel and Gigabit Ethernet.

For the actual transfer medium the standard describes two different connection technologies, one for Copper Cable and one for Fibre Optics [5]. The copper cable connection uses a 24 channel cable and the fibre connection is made for a 12 fibre flat-cable connection. The line port of the SUMAC chip has two selectable operational modes: the optical connection with half the number of lines uses twice the clock frequency. To extend the range of connection the SUMAC line input has a very complex skew suppression circuit that is autoadjusting by a training cycle with a special data pattern and slower clock cycle on one of its two clock signals. The following describes in detail the tests done to come to a working version of the fibre connection for GSN. Some knowledge of the SUMAC chip may be necessary to understand the problems that are handled here in detail.

The SuMAC Chip Line Interface:

First of all there is the note from the developers of the SUMAC chip at SGI that it is very questionable that the optical mode will work at the full clock frequency of 1 GHz needed for the optical (12 bit) mode.

The next question is the clock oscillator itself. The best external oscillator that is commercially available has a frequency of 825 MHz. This is independent from the question how to handle this class of frequencies, via a printed circuit board with all its stray capacities and inductances, into the SUMAC chip, without signal degradation. For

the designers of the SUMAC chip it would only have taken three more Asic gates to make a fixed frequency doubler inside the chip.
The last question is if the optics would ever have worked, as the reference clock given by the SUMAC chip in optical mode is "CLOCK", a signal disturbed by the training cycle bringing the optics out of DC balance (or at least it will disturb the stability of any PLL that may be in the loop).

It was decided at CERN to look at the GSN-Optical problem. The only commercially available components that can handle a 12 bit parallel fibre connection are the Infineon Paroli's. They exist in two versions [8]:

1. A 12 channel wide direct coupled optical converter in versions for 1 Gbaud, 1.6 Gbaud and 2.5 Gbaud. (V23814/15-K1306-M130)
2. A 22 channel multiplexed version available for 200 - 500 Mbits/s per channel. (V23814/15-K1306-M230)

From the problems with the SUMAC chip it is clear that using the 12 bit optical mode with the 12 channel component is a risk. The 24 bit mode foreseen for copper cable connections is a proven concept that is used already in GSN equipment. As a conclusion, the work done for a GSN Optical connection concentrated on the 22 channel multiplexed component coupled to the SUMAC chip working in 22 bit mode.

The Paroli modules use LVDS levels for the data path and LVCMOS for control signals.

Adapting the Paroli to the SUMAC:

In some way the coupling between PECL logic of the SUMAC and the LVDS logic has to be made. These levels look compared to each other as follows:

	SUMAC Chip			Paroli In		
	Min	Typ	Max	Min	Max	unit
Input Common mode Voltage	1.05	1.30	1.55	1.2		V
Differential Input Voltage	0.150	-	2.70	0.1	1	V
Output Common mode Voltage	-	1.25	-	1.2		V
Differential Output Voltage	2.20	2.50	2.70	0.25	0.4	V

In the direction SUMAC to PAROLI we see that:
The Paroli demands a min. -max. differential input signal of 100 - 1000 mV
Where the Sumac chip delivers 2200 mV
Output common mode for the Sumac is 1250 mV
For the Paroli I calculated the common mode at 1200 mV

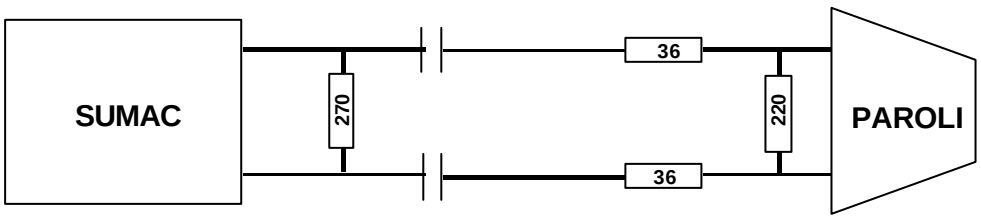

Fig. 1

In order to stay in a safe operating area some adaptation has to be done. It is solved by using the AC coupling of the copper connection and with an attenuating termination as in Fig 1.

The result measured on the clock signal is 800 mV on the PAROLI input pins. Fig 2 gives the waveform for Clock_2 at the input of the Paroli transmitter and fig 3 the same signal at the output of the Paroli receiver.

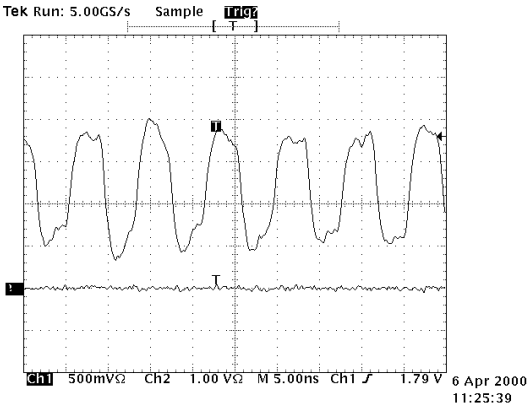

Fig 2

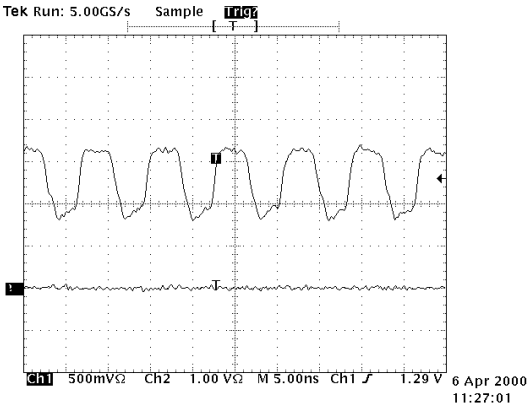

Fig 3

In the direction from Paroli to SUMAC the following data is valid

The Sumac chip demands as diff. input signal minimum		150 mV
The Paroli has a minimum diff. output signal of		250 mV
Input common mode for the Sumac is	± 250 mV	1300 mV
Output common mode for the Sumac is		1250 mV

This makes it possible to use a DC coupling, keeping the 75 ohm Tevenin equivalent terminator resistors as for the cable connection in place.

Output Timing:

Both Transmitter and Receiver synchronise with PLL oscillators, doubling or quadrupling the clock frequency on the fibre, corresponding to the "Clock" or "SCI" mode. The second mode corresponds to the SUMAC functionality.

Due to the PLL's the receiver chip brings clock and the data on phase to the output pins. Such a 1 nsec external clock delay must be made as is given in Fig 4.

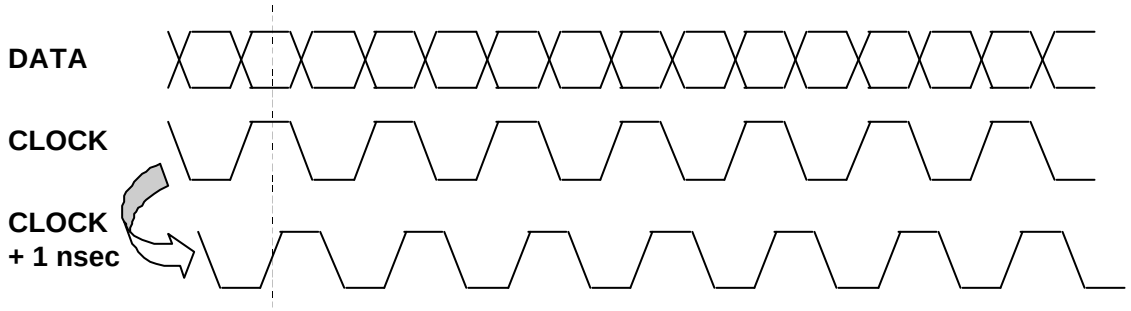

Fig. 4

Test Set-Up:

For the test a small piggyback board with the optical components was made that plugs into the auxiliary connector of the GSN port on a Genroco bridge. The board uses a 5V power supply with a 3.3 V stabiliser. Every separate power group is individually decoupled with a ferrite component and a decoupling capacitor per power pin.
All data lines are paired and calculated for a 75 Ohm impedance. Placing transmitter and receiver on opposite sides of the board, avoids crossings and via's in the data lines.

A PECL clock driver was added in case a second clock had to be generated, or if a divide by 2 effect would occur on one of the clocks. Its final function was to generate a clock delay. The board has only 4 layers. See also Fig 5 for the board and Fig 6 for the test set-up.
As test generator the Genroco test board, a modified FC converter for the bridge is used.

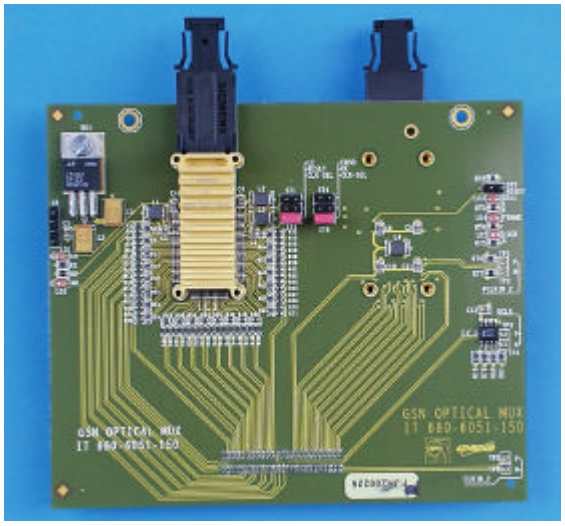

Fig 5

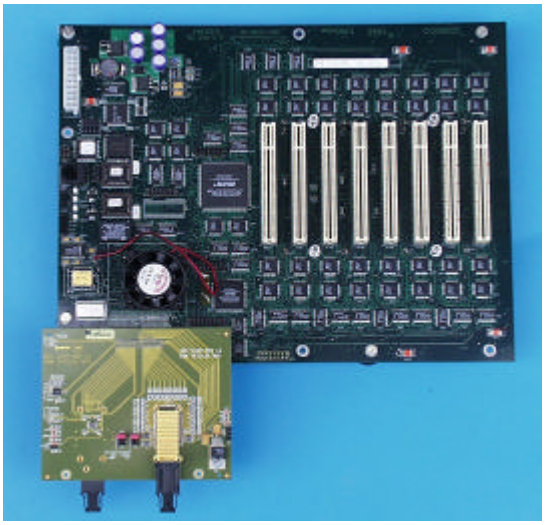

Fig 6

Test Results:

One of the optical transmitters was not working properly so I had only one working board available. This limited the testing to loop-back mode on a single bridge. (It was originally planned to connect two bridges both with a GigE board and run data between them).
It has to be remarked that in this set-up and during these tests Clock_2 has only 270 psec delay. After some initial set-up tests the following results were obtained:

As a first attempt all tests available on with test board were run for about 1 hour with a 5 m fibre and using all VC's.

1. Loop & Check Pings.
2. Loop & Check Single Packet Messages.
3. Loop & Check Multi Packet Messages.

During these tests no error was found. The fibre was opened repeatedly to check that error messages would be given.

This was followed by a long term test using the third test with 25 micropacket messages and using 4 fibres of 5 m each patched together to 20 m. (this is all I have available).
After 8 hours an error occurred in the form of a missing high byte. This error reproduced itself at regular distances. Concentrating the ventilator air-stream to the transmitter circuit (fig 7) solved the problem and the circuit is now working more than 48 hours without any error detected.

Conclusion.

By doing this optical test, CERN is the first place to have a GSN optical connection working. It shows that the Paroli type V23814/15-K1306-M230 is a well working component that can be used for GSN optical connections up to 75 m. It can also be a fast optical connection in HEP experiments with up to 22 channels in a single connection.
According to Infineon, distances of more than 75 m lead to fibre skew problems. For this distance skew tested cables are available.
A critical point with the Paroli components is good cooling, especially for the

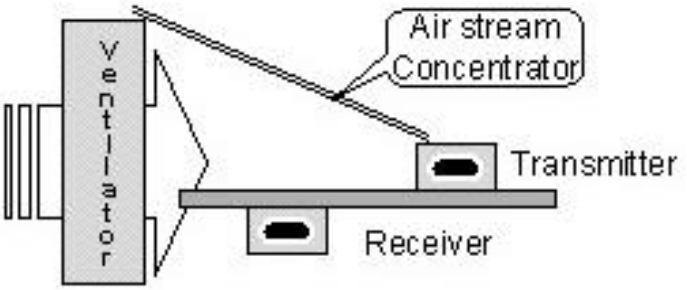

Fig 7.

transmitter.
It should also be noted that the connector guidance pins are inside the component connector. The cable has no such pins. In the case of cable patches these guidance pins have to be placed manually. Infineon proposes a solution that uses extension cables with a male and a female connector.
In order to obtain interoperability between all GSN equipment from different manufacturers, it is necessary that common signal-pin relations get standardised. A proposal is given as an Annex.
Technical documentation of this project was presented at the HNF HIPPI-6400 standardisation meeting of 4 April 2000 in San Diego, USA [7], with the result that the actual version of the HIPPI-6400 OPT standard is withdrawn from public review in NCITS, to be modified with the proposed solution for GSN optical, in the T11.1 group.

Acknowledgement

I want to thank all those who have made it possible to work on the GSN-Optical problem, especially: at CERN, Ben Segal who allowed me the time to do so; at Infineon in Berlin, Germany, Lothar Droege for his technical assitance around the Paroli modules; at Genroco in Slinger, USA, Brian Breuer for technical assistance with problems around the SuMAC chip, and Don Woeltz for presenting my work in the HNF technical meeting in San Diego; and Genroco in general for making GSN bridges and GSN test boards available.

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[3] Scheduled Transfer Protocol (ST), T11.1/Project 1245-D/Rev 3.2, ANSI NCITS xxx-199x., ISO/IEC 11518-xx. http://www.hippi.org/cST.html

[4] SCSI on Scheduled Transfer (SST), ANSI NCITS xxx-199x., ISO/IEC 11518-xx, http://www.hippi.org/cSCSI.html

[6] HIPPI-6400-OPT Rev 1.2, ANSI NCITS xxx-199x., ISO/IEC 11518-xx., http://www.hippi.org/c6400OPT.html

[7] HIPPI ad-hoc Optical Working Group Minutes, San Diego, 4 April 2000. http://www.hippi.org/min 0004opt.pdf.

[8] Data sheets for Infineon Paroli components can be found on the web at the following URL: http://www.infineon.com/products/fiber/index_paroli.htm

ANNEX

Proposal for Paroli DC standard pin Pin Connections

SUMAC_Out FUNTIONS	Paroli PIN No	DC TX Function	DC RX PIN No	SUMAC_In FUNTIONS
	1	Vcc 1	Vee	
	2	t.b.l.o.	Vcc 1	
	3	t.b.l.o.	Vcc 2	
	4	t.b.l.o.	t.b.l.o.	
	5	t.b.l.o.	-RESET	
	6	LA	Frame-Det	
	7	Vee	Vcc 3	
	8	Vee	Vee	
	9	Vcc 3	Vcc 4	
	10	MA	Lock-Det	
Clock2_Out_L	11	CI N	CO P	Clock2_In_H ([1]
Clock2_Out_H	12	CI P	CO N	Clock2_In_L ([1]
D08_Out_L	13	DI 01 N	DO 01 P	D08_In_H
D08_Out_H	14	DI 01 P	DO 01 N	D08_In_L
D09_Out_L	15	DI 12 N	DO 12 P	D09_In_H
D09_Out_H	16	DI 12 P	DO 12 N	D09_In_L
D00_Out_L	17	DI 02 N	DO 02 P	D00_In_H
D00_Out_H	18	DI 02 P	DO 02 N	D00_In_L
D10_Out_L	19	DI 13 N	DO 13 P	D10_In_H
D10_Out_H	20	DI 13 P	DO 13 N	D10_In_L
D01_Out_L	21	DI 03 N	DO 03 P	D01_In_H
D01_Out_H	22	DI 03 P	DO 03 N	D01_In_L
D11_Out_L	23	DI 14 N	DO 14 P	D11_In_H
D11_Out_H	24	DI 14 P	DO 14 N	D11_In_L
	25	Vcc 3	Vcc 4	
D02_Out_L	26	DI 04 N	DO 04 P	D02_In_H
D02_Out_H	27	DI 04 P	DO 04 N	D02_In_L
	28	Vee	Vee	
D12_Out_L	29	DI 15 N	DO 15 P	D12_In_H
D12_Out_H	30	DI 15 P	DO 15 N	D12_In _L
D03_Out_L	31	DI 05 N	DO 05 P	D03_In_H
D03_Out_H	32	DI 05 P	DO 05 N	D03_In_L
D13_Out_L	33	DI 16 N	DO 16 P	D13_In _H
D13_Out_H	34	DI 16 P	DO 16 N	D13_In _L
D04_Out_L	35	DI 06 N	DO 06 P	D04_In_H
D04_Out_H	36	DI 06 P	DO 06 N	D04_In_L
D14_Out_L	37	DI 17 N	DO 17 P	D14_In _H
D14_Out_H	38	DI 17 P	DO 17 N	D14_In _L
D05_Out_L	39	DI 07 N	DO 07 P	D05_In_L
D05_Out_H	40	DI 07 P	DO 07 N	D05_In_H
D15_Out_L	41	DI 18 N	DO 18 P	D15_In_L
D15_Out_H	42	DI 18 P	DO 18 N	D15_In_H
D06_Out_L	43	DI 08 N	DO 08 P	D06_In_L

D06_Out_H	44	DI 08 P	DO 08 N	D06_In_H
	45	Vee	Vee	
C2_Out_L	46	DI 19 N	DO 19 P	C2_In_H
C2_Out_H	47	DI 19 P	DO 19 N	C2_In_L
	48	Vcc 3	Vcc 4	
D07_Out_L	49	DI 09 N	DO 09 P	D07_In_L
D07_Out_H	50	DI 09 P	DO 09 N	D07_In_H
C3_Out_L	51	DI 20 N	DO 20 P	C3_In_H
C3_Out_H	52	DI 20 P	DO 20 N	C3_In_L
C0_Out_L	53	DI 10 N	DO 10 P	C0_In_L
C0_Out_H	54	DI 10 P	DO 10 N	C0_In_H
Frame_Out_L	55	DI 21 N	DO 21 P	Frame_In_L
Frame_Out_H	56	DI 21 P	DO 21 N	Frame_In_H
C1_Out_L	57	DI 11 N	DO 11 P	C1_In_L
C1_Out_H	58	DI 11 P	DO 11 N	C1_In_H
CLOCK_Out_L	59	DI 22 N	DO 22 P	CLOCK_In_H
CLOCK_Out_H	60	DI 22 P	DO 22 N	CLOCK_In_L
	61	CLK-SEL	CLK-SEL	
	62	t.b.l.o.	o.e.	
	63	Vcc 3	t.b.l.o.	
	64	-RESET	Vcc 4	
	65	Vee	Vee	
	66	Vee	Vcc 3	
	67	LE	-SD 11	
	68	-LE	ENSD	
	69	t.b.l.o.	t.b.l.o.	
	70	t.b.l.o.	Vcc 2	
	71	t.b.l.o.	Vcc 1	
	72	Vcc 1	Vee	