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HIPPI Developments for CERN experiments

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Abstract

Standard, fast, simple, inexpensive; is this not a contradiction in terms? The High-Performance Parallel Interface (HIPPI) is a new proposed ANSI standard, using a minimal protocol and providing 100 Mbyte/sec transfers over distances up to 25 m. Equipment using this standard is offered by a growing number of computer manufacturers. A commercially available HIPPI chipset allows low cost implementations. In this article a brief technical introduction to the HIPPI will be given, followed by examples of planned applications in High Energy Physics experiments including the present developments involving CERN: a detector emulator, a risc processor based VME connection, a long distance fiber optics connection, and a HIPPI testbox.

A high throughput point-to-point connection

High Energy Physics experiments have an impressive requirement for high bandwidth data transfers between scattered locations, to handle both the second-level trigger and event building. General purpose busses or links are not able to provide these high-speed transfers, and we assume that it should be possible to use synchronous unidirectional links to transfer the data from one point to another. We also assume that we will use a growing number of components supplied by industry; therefore it is important to choose a link that has the support of the major computer and peripheral manufacturers.

HIPPI

We have decided to use the High Performance Parallel Interface (HIPPI) to implement these links. The HIPPI specification was started in the Los Alamos laboratory in 1989 and is now a proposed ANSI standard (X3T9/88-127, X3T9.3/88-23, HIPPI PH) [1,2]. This standard allows 100 Mbyte/sec synchronous data transfers between a "Source" and a "Destination". Seen from the lowest level upwards the HIPPI specification proposes a logical framing hierarchy where the smallest unit of data to be transferred, called a "burst" has a standard size of 256 words of 32 bit or optional 64 bit (Fig. 1).

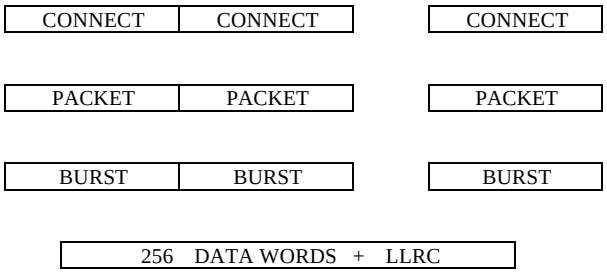

Fig. 1: Logical framing hierarchy

However the size of a burst may be as small as 1 word only. Error checking adds 4 parity bits to each 32 bit word and one "LLRC" word that implements a lateral parity at the

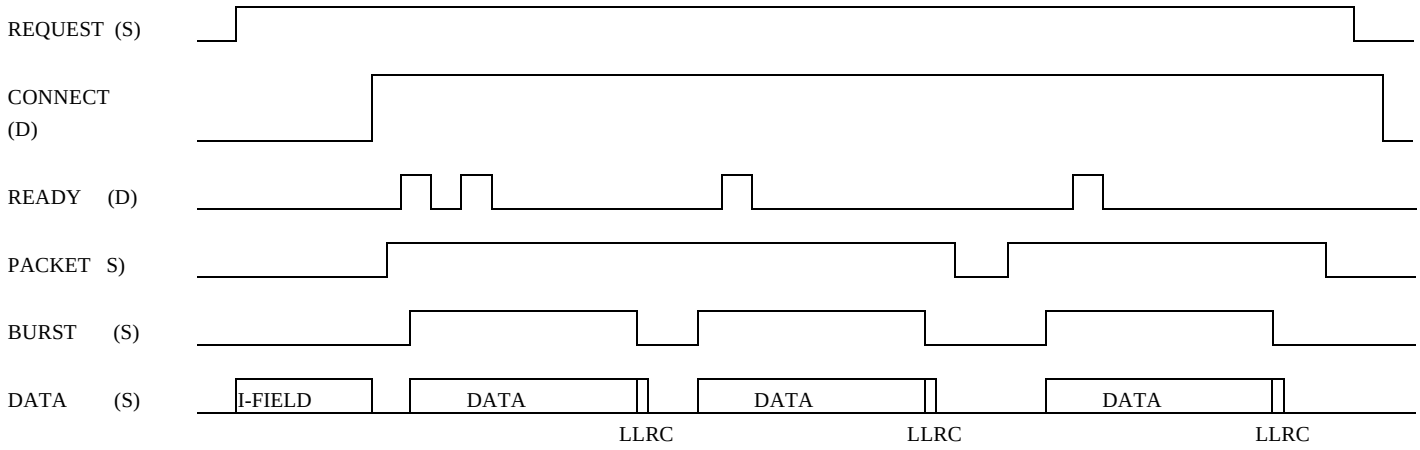

Fig 2: A Typical HIPPI Sequence

end of each burst. For each burst to be sent by the source, the destination needs to acknowledge in advance with a "ready" pulse. One or more bursts are combined in a "packet" without a given upper limit. To avoid partly empty bursts, one shorter than the prescribed size can be included in each packet. The same structure repeats for the "connect cycle" where the number of packets per cycle can be chosen freely. To establish a connection the source sends a "request" to the destination which should acknowledge with a "connect" signal. Data put on the datalines during thisrequest-connect handshake can be used to send information concerning data to be transferred, or can be used as a addressing information in the case a switch is used, and is called the "I-field" (Fig. 2). Data transfer uses a 50 twisted pair cable of 15m or 25m. The clock is transferred through the cable with the data and has a rate of 25 Mhz which results in 100 Mbyte/sec synchronous data transfers. An optional second cable can double this throughput.

A HIPPI chip set

A silicon chip-set in the form of a source circuit and a destination circuit are commercially available from AMCC. This chips perform the hardware protocol encoding and decoding and interface at the HIPPI-PH level, including burst partitioning of the input data. The data inputs on the source and outputs on the destination are foreseen to interface with synchronous FIFOs. The ECL conversions for connection to the cable are done inside the chips. The destination chip uses a phased lock loop to resynchronize the clock, which is necessary for applications in switches. These chips have been successfully used in several applications.

Commercially Available Products

HIPPI interfaces are commercially available from a growing number of computer manufacturers as: IBM for the IBM 3090 and NEC mainframes, Sun and Silicon Graphics for workstations. Network Systems Corporation has a VMEbus to HIPPI interface and makes a HIPPI crossbar switch. The latter has eight simplex channels or four full duplex channels and uses the bits 0-23 of the I-field for routing. The least 4 bits are the actual output port address. They are taken out by passing the switch and bits 4 to 23 are shifted to the low end. The actual switch address is placed in the upper 4 bits just freed. In this way several crossbar switches can be cascaded while the path followed can be reconstructed by the final destination. As an option the I-field can be passed unchanged.

HIPPI for LHC

For Large Hadron Collider (LHC) experiments the very high interaction rate and the enormous number of channels present severe problems in storing and moving data at all levels of the trigger and data acquisition chain. Several study projects for new detector and trigger logic have been approved by the Detector Research and Development Committee (DRDC).

Detector Emulator

The Detector emulator, known now as SLATE is designed to provide data at a rate, and a complexity, that allow realistic tests of the performance of links and processors chosen for use in a second level trigger. Flexibility is obtained by using software to create files of data describing the output of the detector. To make tests of different architectures as realistic as possible physics generators and detector simulations are used to produce a data-base. A workstation is used to construct from this data-base and from additional user data, the files containing the regions of interest. After formatting and adding the parameters for the physical output, this files are loaded into the emulator using ethernet. On receipt of a start signal the emulator loops sending partial event data. Hardware daughter boards are used as output device such that different physical outputs can be tested.

The emulator system is being build in VME. Basically it is a memory which size is defined as 48 bit by 64 Kwords. Information from simulations of the Spacal and TRD detectors indicate that areas of interest for second level triggers have the size of about 2 Kbyte. Using two units 500 events can be stored. To achieve the necessary transfer time of 10 μsec/event, data must be transported at a rate of 100 Mbyte/sec.

The first daughter board to be tested is a HIPPI source[4]. It uses the AMCC source chip.

VMEbus to HIPPI interfacing

The VMEbus to HIPPI interface is designed to allow the integration of HIPPI into VMEbus environments. VMEbus has been selected by the DRDC project as RD13 and is a framework in which to prototype new hardware and software. In RD13 it is planned to use the commercially available HIPPI switch from NSC to build events. The idea of using a crossbar switch to build events is presented in a paper by E. Barsotti et al.[5]**.** In the RD13 project each detector crate will be equipped with an intelligent HIPPI source going to the crossbar switch to build the event in one of several destinations [6]. The on board processors will analyze the data and good events are transmitted to the host computer.

For the HIPPI sources the RIO 8260 processor board with a RISC R3051 microprocessor, equipped with a RIO HIPPI Source daughter board, will be used. The RHS module implements a HIPPI Source interface that is fully compliant with the HIPPI-PH standard. The processor sets up all data transfers and sends data from either the VME-bus or the local memory to the RHS. The RIO 8260 has a special mode to transfer data from the local memory to the RHS at a rate of 50 MByte/sec. The device has selectable modes to swap the bytes in the datawords, a feature needed if one sends data to computers with a different byte organization.

For debugging and testing purposes, the RHS has a step-by-step mode and is equipped with registers that can read back all data and control signals under software control.

HFOX

One of the first applications at CERN for HIPPI components will be in the L3 off-line area [7]. It is planned to attach several workstations via a HIPPI switch to an IBM 3090/200j system (Fig. 3:). This data analyzing system is for

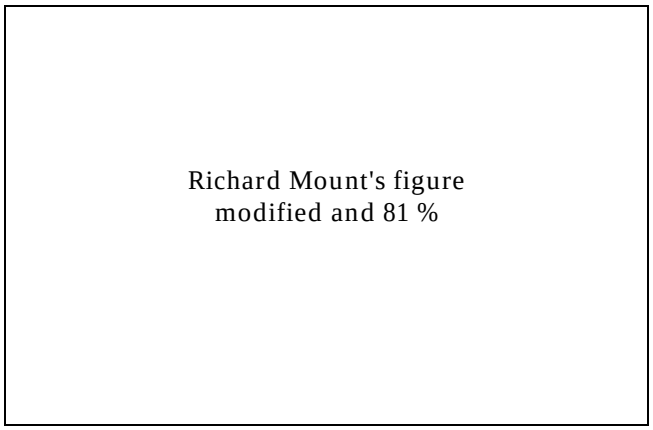

Fig. 3: The L3 Pilot Project

the moment coupled to the on-line VAX 6300 data acquisition computer using a 10 Km fiber optic link running at 1 Mbyte/sec . To cover this distance with an increased speed we are developing the **H**IPPI **F**iber **O**ptic e**X**tension (HFOX) full duplex connection that replaces the standard 25 m copper cables.

For serialization and deserialization of the 43 HIPPI signals the Hewlett-Packard chipset (table 1) is used [7]. This bipolar silicon chipset is specified for 16 bit parallel input at 75 Mhz and delivers with the encoding overhead a 1.5 Ghz serial output. The proprietary encoding algorithm achieves a good long term DC balance which simplifies stabilization of the laser-bias for constant output power. The interface to this chipset is a 1 to 3 multiplexer for the source coupling. The 25 Mhz HIPPI clock is used as input to the chipsets 75 Mhz phase locked loop. In the receiver the balanced code permits AC-coupling without signal degradation. The data is demultiplexed 3 to 1 to recombine the 43 bits and divides the extracted clock down to the original 25 Mhz. HFOX is a collaboration between CERN, Birmingham University and Hewlett Packard England.

CHIP	FUNCTION	SIZE IN mm	POWER
Encoder	Encoding 16 : 4 multiplex	4 x 5	3 W
MUX	4 : 1 multiplex	1.3 x 2	1 W
PLL	Clock recovery 1 : 4 demultiplex	2.3 x 2.6	1.5 W
Decoder	Decoding 4 : 16 demultiplex	4 x 4	2 W

Table 1 H.P. Chip set

Data Generator	Variable Timings	Error Detection	Analysis
Cyclic Data	Switch Interconnect	Inject Parity Errors	Connect Length
Random Data	Request Timing	Inject LLRC Errors	Ready Length
1024 Data Words	Connect Accept Time		Interconnect D-S
	Ready Accept Time		Ready Counter
Data Format	Valid Connect to Packet		Variable Clock Delay
Set Packet Length	Packet to Burst		**Clock Analysis**
Set Burst Length	Burst Interval		Variable Frequency
Change I-field	Output Clock Delay		Duty-Cycle Jitter
			Frequency Jitter

All functions of the HIPPI source can run manually in single cycle mode,
or under processor control with programmed cycle speed.

Table 2 HIPPI Testbox Source Properties

The HIPPI Testbox

Tp allow CERN to test and maintain HIPPI equipment, a powerful test facility is required. A tester has been developed at Los Alamos National Laboratories. A second testbox is being constructed at CERN. This testbox allows testing HIPPI equipment both inside and outside the specifications [10,11] and includes the facility of deliberately introducing errors. The main features of the CERN HIPPI testbox are:

Manual set-up
Processor controlled set-up
Possibilities for remote analysis
Checking the HIPPI specifications
Checking not allowed conditions

Separate source and destination boards, can be used individually to test HIPPI equipment, or the boards may be connected and the testbox can placed in an existing link. Using the VME interface for processor control gives an extended range of possibilities and makes more accurate adjustments possible. Coupling the processor to Ethernet makes remote analysis possible. The remote control software will use TCP/IP. The user interface uses X-windows. The host machine will be a UNIX workstation. Analysis can be done from a large amount of workstations including the more sophisticated PC's. For source and destination the functionality can be divided in four subgroups, Data, Variable timings, Error detection and Analysis. The source (Table 2) cyclic and random data generator is a hardware implementation able to deliver data at the full HIPPI speed. The 1024 x 40 Fifo memory is loaded with data via the VME port. The destination has the same size Fifo memory to store received data together with the Analysis bits. Variable timings on source, and destination (Table 3) are settings running from 0 to 15 or from 0 to 31 clock pulses for the indicated functions. Each has a default setting that corresponds to the minimum value in the specifications. The error detection part in the source can inject parity bits in every byte and LLRC errors on every bit and in any word chosen. The destination will store the error bits. Counters register up 256 errors for long term tests. The analysis part are functions used for remote analysis. However Clock Analysis has only manual controls and is used for clock stability and benchmark tests.

The HIPPI testbox is being build using VXI crate and boards. To avoid timing constraints it is almost entirely

Stored Data	Variable Timings	Error Detection	Analysis
I-field	Switch Interconnect	Detect and Store Parity Errors	Start of Packet
1024 Data Words	Reject/Connect cycle	Count Parity Errors	End of Packet
	Connect to Ready	Detect and Store LLRC Errors	Start of Burst
	Ready Pulse Length	Count Parity Errors	End of Burst
			Interconnect S-D

Table 3 HIPPI Testbox Destination Properties

constructed with ECL logic. The design work on the source is almost finished. The destination prototype is on the testbench. It is hoped to have the complete prototype working in the beginning of 1992.

Conclusion

HIPPI is a new standard for fast point to point connections. It has a simple protocol which can almost completely be executed in hardware, keeping software overhead low. Interfaces are commercially available from several mainframe and workstation manufacturers. A commercially available crossbar switch can give network like flexibility and can be useful in event building. A chipset is available as an industry product. The present distance limit of only 25 m can be extended by replacement of the cable with a serializer and deserializer interconnected with fast fiber optics to reach 10 km or more. VMEbus systems are being interfaced to HIPPI. Using this HIPPI components, fast point to point connections can solve many of the data transport problems for data acquisition in the coming generation of high energy physics experiments.

Acknowledgement

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References:

[1] High Performance Parallel Interface. Mechanical, Electrical and Signalling Specification (HIPPI PH) X3T9/88-127 X3T9.3/88-023 Rev 8.1 23 June 1991

[2] The High Performance Parallel Interface (HIPPI) and Ultra Speed Networks.
Don Tolmie Los Alamos National Laboratory USA
American Institute of Physics 1990

[3] Embedded Architectures for Second-Level-Triggering in LHC Experiments (EAST)
R.K. Bock & al. CERN/DRD/90-56 DRDC/P12
30 October 1990

[4] HIPPI Source Board
T. Anguelov, E. van der Bij. R. McLaren, A. van Praag
CERN/EAST/note 91-12 in preparation

[5] A scalable data taking sytem at a testbeam for LHC.
L. Mapelli*, P. LeDu, J. Harvey, E. Valente

[6] Effects of various event building techniques on data acquisition system architectures
E Barsotti, A. Booth, M. Bowden Fermilab
AIP Conference Proceedings 209 1990

[7] Use of HIPPI/Fibre Channel to Build an Integrated Computing Environment
R.P.
Mount California Institute of Technology Pasadena,
L3 Experiment CERN Geneva Switzerland
30 November 1990

[8] A 1.5 Gb/s Link Interface Chipset For Computer Data Transmission
R. C. Walker, T. Hornak, C.S. Yen, J. Doernberg,
K. Springer
Instruments and Photonetics Laboratory HPL-90-105
July 1990

[9] Testing and Benchmarking of HIPPI Interfaces
A. van Praag CERN ECP/EDU/DQ/

[10] A Development System for the High Performance Parallel Interface (proposal)
A. van Praag CERN ECP/EDU/DQ/