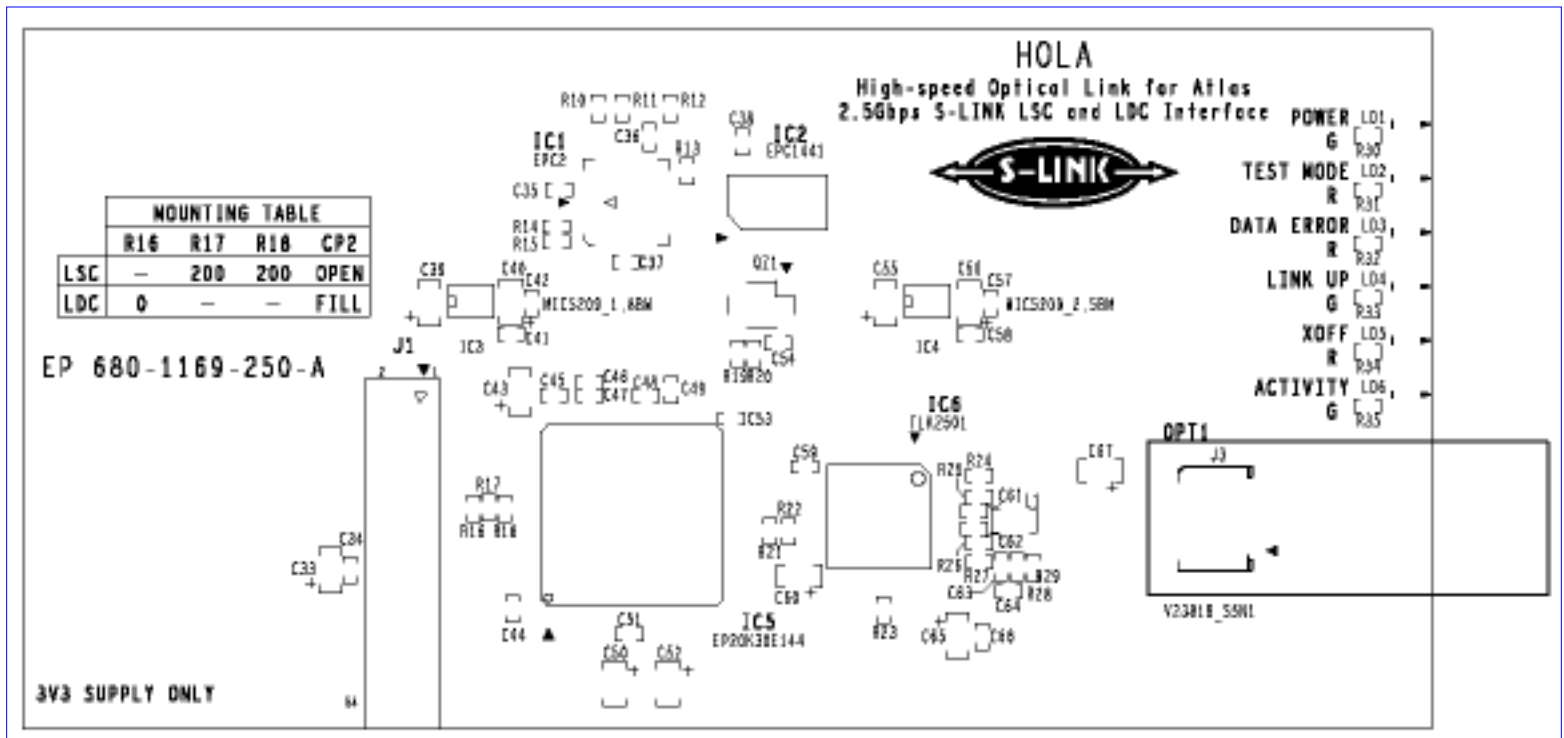




HOLA

High-speed Optical Link for Atlas

2.5 Gbps S-LINK LSC and LDC S-LINK Interface



(Circuit number EP680-1169-250)

DESCRIPTION

The HOLA S-LINK interface is a standard [S-LINK](#) implementation which uses the TI TLK2501 2.5 Gbps transceiver both for the forward and for the return channel (one per card). For the optical transmission Small Form Factor Pluggable (SFP) Multimode transceivers with LC Connector are used.

As opposed to the [ODIN](#) S-LINK, the HOLA can transfer with one duplex fibre at the full S-LINK bandwidth of 160 MB/s. Furthermore the HOLA will be cheaper than the ODIN.

The design is not intended to be used in an environment with radiation.

General features

- Duplex S-LINK
 - 32-bit data width
 - UCLK up to 40 MHz
 - 125 MHz link clock
 - 160 MBytes/s maximum data rate
 - 125 MBytes/s transmission rate for control information (UCTRL# low)
 - 31.25 MHz sampling rate for the return lines
 - Block basis error reporting on data words
 - Word-by-word error reporting on control words
 - 3.3V supply voltage
 - Autonomous link synchronization and maintenance of physical link
 - Improved S-LINK Reset protocol
 - Test function for the return lines
 - Flow control is provided both in data mode and self test modes
 - only one duplex fibre needed for full S-LINK bandwidth of 160 MB/s
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STATUS

<i>10 October 2001</i>	Hardware specification ready
<i>1 March 2002</i>	Schematics ready and reviewed by Peter Jansweijer/NIKHEF and Tivadar Kiss/CERNTECH. PCB design will start 7 March.
<i>11 April 2002</i>	PCB design finished. 16 boards ordered (5 prototype links and 6 empty PCBs for NIKHEF MDT)
<i>24 April 2002</i>	Empty PCBs will arrive 20 May (delays in ordering because of holidays and miscommunication)
<i>15 May 2002</i>	18 empty PCBs arrived
<i>28 May 2002</i>	6 boards mounted. Found problem with padstack TLK2501 (IC smaller than pads). No problem for debugging, but needs re-layout for series production.

DOCUMENTATION

- CERN Engineering Data Management System (EDMS)
 - [S-LINK project](#)
 - [HOLA](#)
 - HOLA Hardware specification
 - [html](#)
 - HOLA data sheet
 - [html](#)
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CONTACTS

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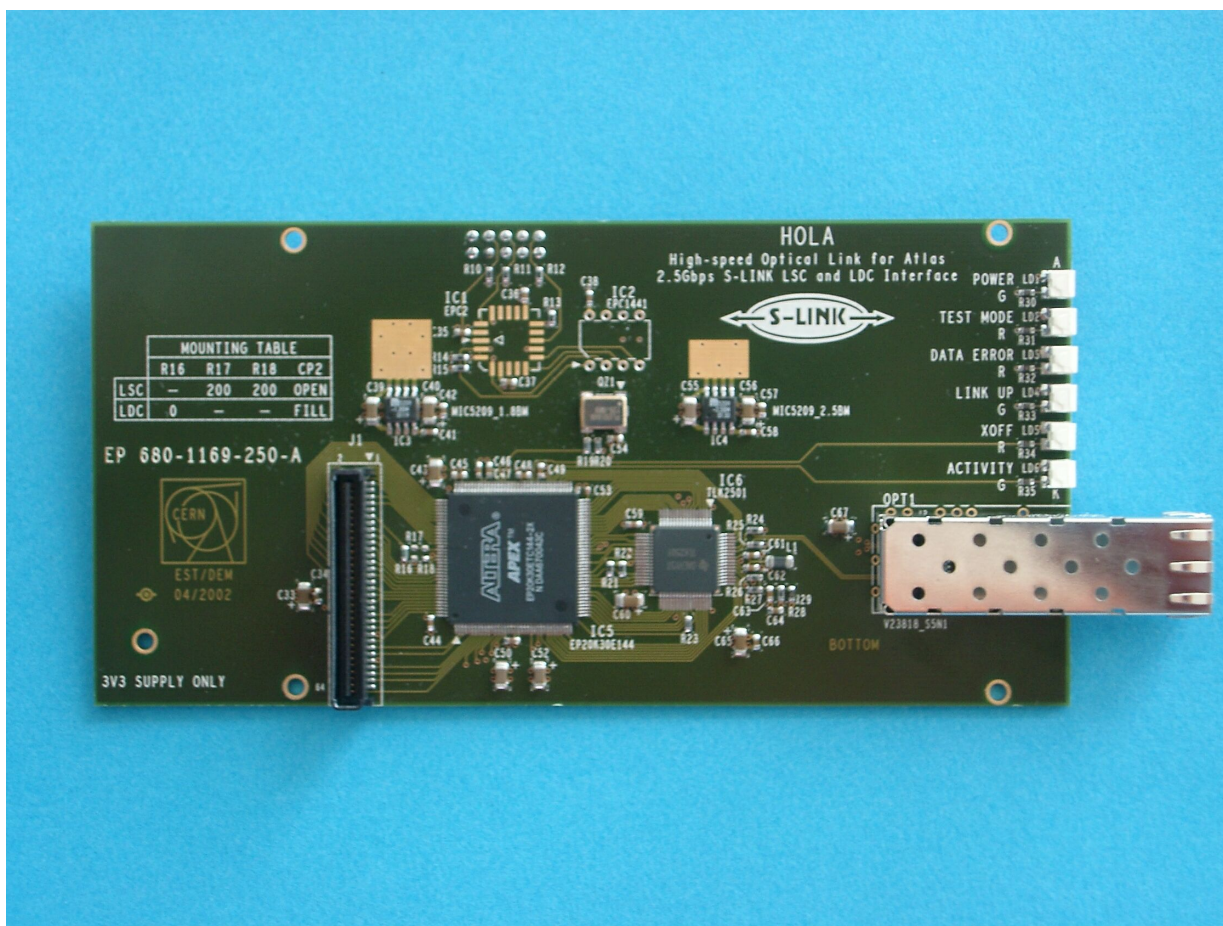
[CERN](#) - [High Speed Interconnect](#) - [S-LINK](#)

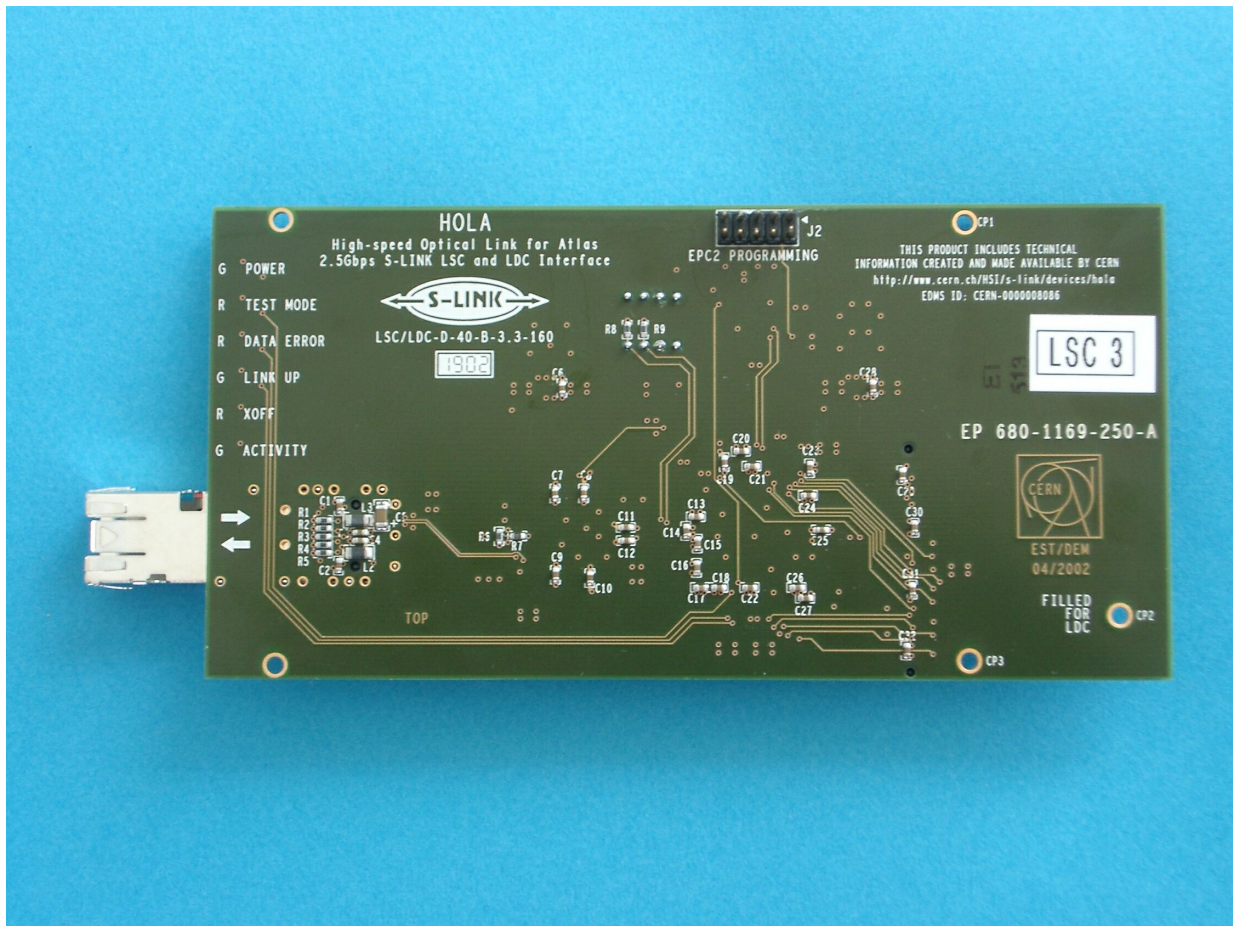
[Aurelio Ruiz](#) & [Erik van der Bij](#) - 28 May 2002

HOLA S-LINK Interface Data Sheet

LSC/LDC-D-40-B-3.3-160

Version 1.0





1. Introduction

The HOLA S-LINK interface is a standard S-LINK implementation which uses the TI TLK2501 2.5 Gbps transceiver both for the forward and for the return channel (one per card). For the optical transmission Small Form Factor Pluggable (SFP) Multimode transceivers with LC Connector are used. HOLA S-LINK can transfer with one duplex fibre at the full S-LINK bandwidth of 160MB/s.

More information, including this document, about the HOLA Interface can be found on the World Wide Web at:

<http://www.cern.ch/HSI/s-link/devices/hola/>

The reader of this document should know the basics of the S-LINK specification. This data sheet only points out a few important features of HOLA and makes a few clarifications. The S-Link specification can be downloaded from the Worldwide Web at:

<http://www.cern.ch/HSI/s-link/spec/>

2. Main Features

The S-LINK code for the HOLA cards is:

LSC/LDC-D-40-B-3.3-160

The main features of the HOLA S-LINK implementation are:

General features

- Duplex S-Link
- 32-bit data width
- UCLK up to 40 MHz
- LCLK 40 MHz
- 160 MByte/s maximum data rate
- 125 MByte/s transmission rate for control information (UCTRL# low)
- 15.5 MHz sampling rate for the return lines
- 3.3V supply voltage
- Block basis error reporting on data words
- Word-by-word error reporting on control words
- Autonomous link synchronization and maintenance of physical link
- Test function for the return lines
- Autonomous link synchronization and maintenance of physical link
- Improved S-LINK Reset protocol
- Flow control is provided both in data mode and self test modes
- Only one duplex fibre needed for full S-LINK bandwidth of 160 MB/s
- Optical output, max. cable length with 50µm multimode cables: 300m

3. Installation

Fix the HOLA S-LINK cards with screws to standoff pillars and front panel mounting holes to avoid mechanical stress and contact problems. For proper operation the board should be fixed by all four screws. Avoid mechanical stress on the cards during mounting. Do not plug in and out the cards on the motherboard when this is powered on.

Connect the optical fiber or electrical cable and after powering up the cards the link goes up immediately and Power and Link up leds go on. There is no need for a reset at power up as the cards go up when powered on and fibers are connected.

4. Operating Conditions

Symbol	Description	Min	Typical	Max.	Units
$I_{cc,d-LSC}$	Current drawn	430	540	560	mA
$I_{cc,d-LDC}$	Current drawn	430	580	640	mA
V_{cc}	Voltage LDC	3	3.3	3.6	V
V_{cc}	Voltage LSC	3	3.3	3.6	V
T_{op}	Temperature	0	25	70	C

Table 4-1 HOLA operating conditions

5. Timing characteristics

Table 5-1 gives the required timing parameter for LSC for proper operation. See [1] for explanation of the parameters.

Symbol	Description	Min	Max	Units
t_{DS}	Data Set-up time	10		ns
t_{DH}	Data Hold time	1		ns
t_{ENS}	Enable Set-up time	10		ns
t_{ENH}	Enable Hold time	1		ns
t_{WFF}	Write Clock to Full Flag		12	ns
t_{CLK}	Clock Cycle time	25		ns

t_{CH}	Clock High time	11	ns
t_{cl}	Clock Low time	11	ns

Table 5-1 LSC timing parameters

Table 5-2 gives the guaranteed timing parameters for LDC.

Symbol	Description	Min	Max	Units
t_{DS}	Data Set-up time	10		ns
t_{DH}	Data Hold time	1		ns
t_{ENS}	Enable Set-up time	10		ns
t_{ENH}	Enable Hold time	1		ns
t_{WFF}	Write Clock to Full Flag		12	ns
t_{CLK}	Clock Cycle time	25		ns
t_{CH}	Clock High time	11		ns
t_{CL}	Clock Low time	11		ns

Table 5-2 LDC timing parameters

6. Optical characteristics

Symbol	Description	Min	Typical	Max.	Units
	Link length (50/125 microns)	0.5		300*	m
	Link length (62.5/125 microns)	0.5		200	m
BER	Bit Error Rate			10^{-12}	

lambda	Center wavelength	830	850	860	nm
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Table 6-1 Optical characteristics

(*) Maximum optical length is 400 m, limited to 300 m by the FIFO in LDC (see chapter 12)

7. LED Indicators

Apart from the S-Link specified LEDs, HOLA cards contain an extra LED (ACT - Activity LED). This LED will be illuminated when a write operation was performed on the FIFO in the previous 2^{14} clock cycles. For the LSC, that means approx. 410 us, for a 40 MHz UCLK clock. For the LDC, that means 131 us.

Furthermore, ERR LED on the LSC is active (unused in the S-LINK specification), and will indicate that the FIFO is completely full, because the user has tried to write more than the 32 words allowed after LFF# set.

LED symbol	Color	Function at LSC	Function at LDC
PWR	green	Power On	Power On
TST	red	Self test Mode	Self test Mode
ERR	red	FIFO full	Data Error/ FIFO full
UP	green	Link Up	Link Up
XOF	red	Link Full Flag	Flow control active
ACT	green	Activity	Activity

Table 7-1 LSC and LDC LED indicators

8. User Data Width Lines

The UDW input lines are unused. If HOLA is set to 16 or 8-bit mode the effective transmission rate will go down accordingly since all 32 bits always are transferred.

9. Data Transfer

The HOLA S-LINK will transfer all input data when up, Power and Link Up LEDs are on and LDOWN# lines are high on both sides. If data is written to an LSC faster than 40 MHz the LFF# flag may go low and the XOFF led goes on at the LSC, even if there is no flow control sent from LDC. This is because maximum data transmission rate is 160 Mbytes/s.

The by the S-LINK specified two words after LFF# being asserted are modified. Up to 32 more words can be written to an HOLA LSC after LFF# goes low.

For small data block sizes the LFF# line will also become active as error detection and S-LINK control words take up bandwidth.

10. S-LINK Reset

The HOLA S-LINK features an improved reset protocol, which is compatible to the protocol as described in [1]. The user may reset the whole link from either side, or even both sides. The card reset is changed into a link reset to make the reset an easy and reliable operation.

If the link is down prior to the reset cycle, LDC will come up before LSC, regardless of which side the reset is performed. This eliminates the chance of data written to LSC being lost when the LDC is still down.

If the link is up prior to the reset cycle, the card where URESET# line is asserted will go down according to [1]. The other side will be reset without going down.

It is not recommended to perform a reset while writing data to the LSC, as this will cause data loss.

11. Test Mode

Self-test mode in the forward channel fully complies with S-LINK specification. Furthermore, test mode is also performed on the return channel. An error in the return channel will force the LSC to send continuously wrong test words, causing an error on the LDC.

12. Flow Control

The LDC includes a 512-word FIFO. A flow control request will be sent when more than 256 words are stored, and not directly when XOFF# coming from the Read-Out motherboard (ROMB) is set. Therefore, the ROMB does not need to compensate the reaction time of the whole link, but only the response time of the LDC. This margin introduces a constraint for the maximum cable length. For a buffer of 256 words the maximum length, as calculated below, is 300 m.

The maximum cable length can be calculated from the formula given in [1]:

$$FM = \left(\frac{LDC_{rt} + [L \times UFD \times 2] + LSC_{rt}}{DTR} \right)$$

Where:

RBS = FIFO margin (words)

LDC_{rt} = LDC reaction time to send XOFF after FIFO sets full flag (ns).

LSC_{rt} = LSC reaction time to stop transmitting data after XOFF received (ns).

L = Length of S-LINK (m).

UFD = Unit Fibre Delay - time for light to travel 1m in fibre (approx. 6 ns/m).

DTR = Data Transfer Rate (ns/word).

Data words in LSC and LDC pipelines are included in LSC_{rt} and LDC_{rt} respectively.

Symbol	
LDC_{rt}	80
LSC_{rt}	320
UFD	6
DTR	16

Table 12-1 Flow control parameters

13. Return Lines

Return Lines are always functional, even when link is down and during test mode. An internal parity checking logic ensures proper operation of the Return Lines. The sampling rate of the return lines is 15.5 MHz in normal mode and 7 MHz during test mode.

14. Error Detection

HOLA features a CRC-based block error detection and errors are reported in the following control word, as specified in [1].

S-LINK control words uses parity bits as error detection in order to separate data errors from control word errors.

15. Link Down Function

The following events may result the link down signal to be asserted:

1. Reset cycle
2. Self-test mode
3. Local reset, i.e. the LDOWN# is asserted only on the card where URESET# is set low.
4. LSC or LDC is not powered up
5. Broken optical link
6. Fatal error occurred

16. Known Bugs

For the moment there are no known bugs.

References

[1]. O. Boyle, R. McLaren, E. van der Bij, "The S-LINK Interface Specification", <http://www.cern.ch/HSI/s-link/spec/spec/> CERN, 1997.