5-row P2 connector map to two S-LINK LDCs

		Z	A	B	C	D
LDC SLOT A	1	LD3	LD2	Vcc (1)	LD1	LD0
	2	Gnd (2)	LD5	Gnd (1)	Gnd	LD4
	3	LD7	Gnd	(1)	LD6	Gnd
	4	Gnd (2)	LD10	(1)	LD9	LD8
	5	LD14	LD13	(1)	LD12	LD11
	6	Gnd (2)	LD17	(1)	LD16	LD15
	7	LD20	LD19	(1)	Gnd	LD18
	8	Gnd (2)	LD23	(1)	LD22	LD21
	9	LD25	Gnd	(1)	LD24	Gnd
	10	Gnd (2)	LD28	(1)	LD27	LD26
	11	LCTRL#	LD31	(1)	LD30	LD29
	12	Gnd (2)	LWEN#	Gnd (1)	Gnd	UDW0
	13	LCLK	Gnd	Vcc (1)	UDW1	UTDO#
	14	Gnd (2)	LDOWN#	(1)	UXOFF#	URESET#
	15	URL1	LDERR#	(1)	URL0	Gnd
	16	Gnd (2)	URL3	(1)	URL2	Gnd
LDC SLOT B	17	LD3	LD2	(1)	LD1	LD0
	18	Gnd (2)	LD5	(1)	Gnd	LD4
	19	LD7	Gnd	(1)	LD6	Gnd
	20	Gnd (2)	LD10	(1)	LD9	LD8
	21	LD14	LD13	(1)	LD12	LD11
	22	Gnd (2)	LD17	Gnd (1)	LD16	LD15
	23	LD20	LD19	(1)	Gnd	LD18
	24	Gnd (2)	LD23	(1)	LD22	LD21
	25	LD25	Gnd	(1)	LD24	Gnd
	26	Gnd (2)	LD28	(1)	LD27	LD26
	27	LCTRL#	LD31	(1)	LD30	LD29
	28	Gnd (2)	LWEN#	(1)	Gnd	UDW0
	29	LCLK	Gnd	(1)	UDW1	UTDO#
	30	Gnd (2)	LDOWN#	(1)	UXOFF#	URESET#
	31	URL1	LDERR#	Gnd (1)	URL0	Gnd (2)
	32	Gnd (2)	URL3	Vcc (1)	URL2	Vpc (2)

(1) signals defined by standard VME bus specification. On P2 backplane only available on front side

(2) signals defined by VME64x (not xP) specification

If signals are free on row B, ground the following pins (in priority order): B16, B5, B26, B8

The same mapping may be used if the P3 backplane is like a P2 backplane.

5-row P3 connector map to one S-LINK LDC and one LSC (uses P2-type backplane)

		Z	A	B	C	D
LDC SLOT C	1	LD3	LD2	Vcc (1)	LD1	LD0
	2	Gnd (2)	LD5	Gnd (1)	Gnd	LD4
	3	LD7	Gnd	(1)	LD6	Gnd
	4	Gnd (2)	LD10	(1)	LD9	LD8
	5	LD14	LD13	(1)	LD12	LD11
	6	Gnd (2)	LD17	(1)	LD16	LD15
	7	LD20	LD19	(1)	Gnd	LD18
	8	Gnd (2)	LD23	(1)	LD22	LD21
	9	LD25	Gnd	(1)	LD24	Gnd
	10	Gnd (2)	LD28	(1)	LD27	LD26
	11	LCTRL#	LD31	(1)	LD30	LD29
	12	Gnd (2)	LWEN#	Gnd (1)	Gnd	UDW0
	13	LCLK	Gnd	Vcc (1)	UDW1	UTDO#
	14	Gnd (2)	LDOWN#	(1)	UXOFF#	URESET#
	15	URL1	LDERR#	(1)	URL0	Gnd
	16	Gnd (2)	URL3	(1)	URL2	Gnd
LSC SLOT D	17	UD3	UD2	(1)	UD1	UD0
	18	Gnd (2)	UD5	(1)	Gnd	UD4
	19	UD7	Gnd	(1)	UD6	Gnd
	20	Gnd (2)	UD10	(1)	UD9	UD8
	21	UD14	UD13	(1)	UD12	UD11
	22	Gnd (2)	UD17	Gnd (1)	UD16	UD15
	23	UD20	UD19	(1)	Gnd	UD18
	24	Gnd (2)	UD23	(1)	UD22	UD21
	25	UD25	Gnd	(1)	UD24	Gnd
	26	Gnd (2)	UD28	(1)	UD27	UD26
	27	UCTRL#	UD31	(1)	UD30	UD29
	28	Gnd (2)	UWEN#	(1)	Gnd	UDW0
	29	UCLK	Gnd	(1)	UDW1	UTEST#
	30	Gnd (2)	LDOWN#	(1)	LFF#	URESET#
	31	LRL1	NC (3)	Gnd (1)	LRL0	Gnd (2)
	32	Gnd (2)	LRL3	Vcc (1)	LRL2	Vpc (2)

(1) signals defined by standard VME bus specification. On P2-like backplane only available on front side

(2) signals defined by VME64x (not xP) specification

(3) NC: do not connect (corresponds to LDERR# line on LDC connector)

If signals are free on row B, ground the following pins (in priority order): B16, B5, B26, B8

Erik van der Bij - 17 January 2000