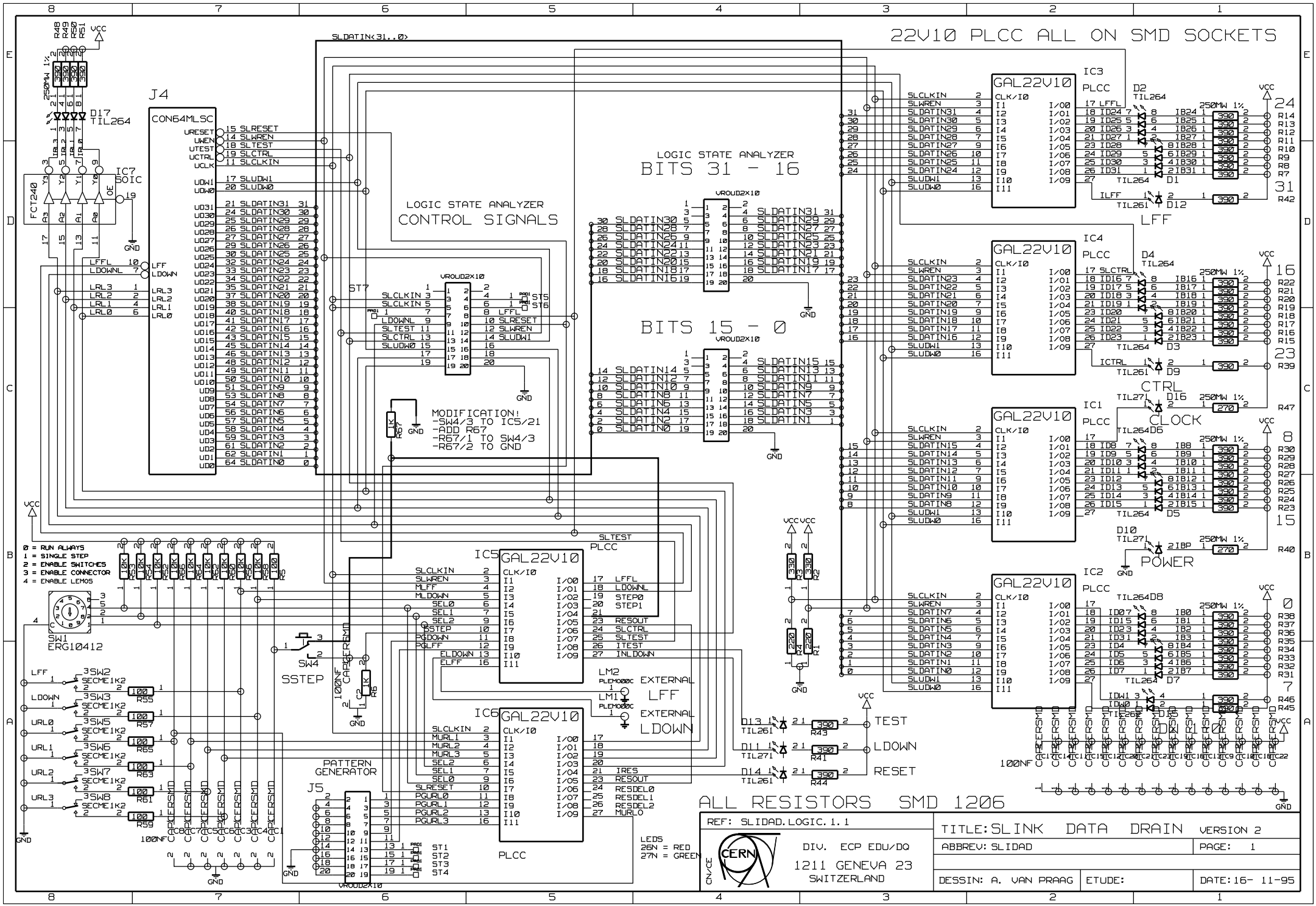
22V10 PLCC ALL ON SMD SOCKETS
LOGIC STATE ANALYZER
BITS 31 - 16
LOGIC STATE ANALYZER
CONTROL SIGNALS
BITS 15 - 0
MODIFICATION!
-SW4/3 TO IC5/21
-ADD R67
-R67/1 TO SW4/3
-R67/2 TO GND
0 = RUN ALWAYS
1 = SINGLE STEP
2 = ENABLE SWITCHES
3 = ENABLE CONNECTOR
4 = ENABLE LEMOS
SSTEP
EXTERNAL LFF
EXTERNAL LDOWN
PATTERN GENERATOR
LEDS
26N = RED
27N = GREEN
ALL RESISTORS SMD 1206
TEST
LDOWN
RESET
LFF
CLOCK
POWER
CTRL
REF: SLIDAD.LOGIC.1.1
DIV. ECP EDU/DQ
1211 GENEVA 23
SWITZERLAND
TITLE: SLINK DATA DRAIN VERSION 2
ABBREV: SLIDAD
PAGE: 1
DESSIN: A. VAN PRAAG
ETUDE:
DATE: 16- 11-95