The S-LINK Interface Specification

Owen Boyle[1], Robert McLaren & Erik van der Bij,
ECP Division, CERN.

1. Also Edinburgh University, Edinburgh, Scotland.

S-LINK specifies a data-link which can be used to connect front-end to read-out at any stage in a dataflow environment. Examples could include sub-detector read-out into an event-builder or channel read-out into a data concentrator.

This specification is indexed by its calendar date (see top left). If you have a hardcopy, please check that it is the most recent version by comparing it with the World-Wide-Web Document on:

http://www.cern.ch/HSI/s-link/

This page intentionally left blank

Table of Contents

1.0 Scope

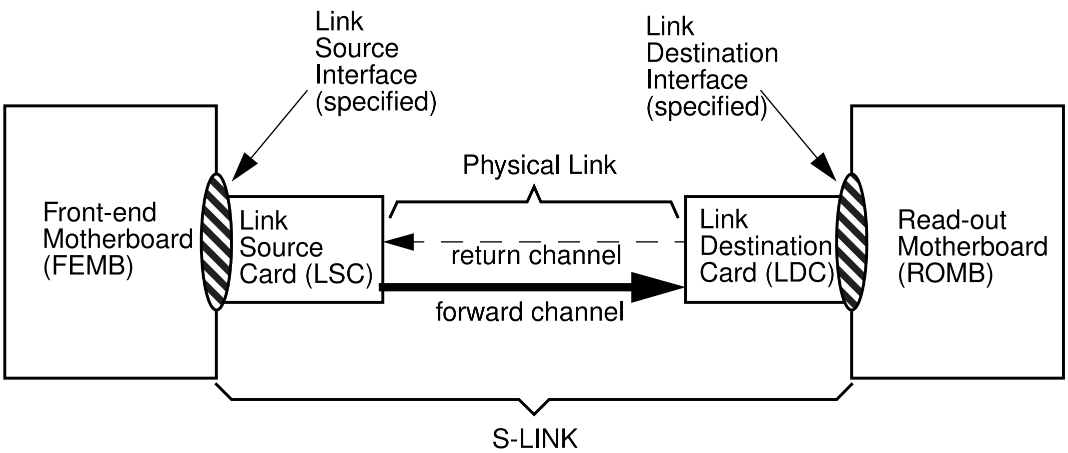
1.1 Description

This specification describes the interface to S-LINK, a Simple Link Interface which can be used to connect any layer of front-end electronics to the next layer of read-out. An S-LINK is a link complying with this specification and can be thought of as a virtual ribbon cable, moving data or control words from one point to another. In addition to simple data movement, S-LINK includes the following features;

- Error detection.
- Return channel for flow control and for return line signals *(duplex version only)*.
- Self-test function.

The specification describes the interface between the Front-end Motherboard (FEMB) and the Link Source Card (LSC) and the interface between the Link Destination Card (LDC) and the Read-out Motherboard (ROMB). It does *not* describe the physical link itself. This concept is shown in Figure 1.

FIGURE 1. The S-LINK concept



In many applications a uni-directional data channel will be required. In other cases the user might require to send flow control and other information back to the FEMB. The S-LINK, therefore, can be constructed in either a *simplex* or a *duplex* version.

In the simplex version, there is no communication path between the LDC and the LSC. That is, data can be sent in one direction only (the forward channel) and data which is transferred to the LSC will be transmitted to the LDC and transferred to the ROMB. An S-LINK of this type could be implemented over a single fibre and is targeted at applications where the number of read-out channels is very large (perhaps several thousand). The immediate consequence of this is that no flow control is possible and every word transferred to the LSC will subsequently be transferred out by the LDC. The user *should* therefore ensure that the ROMB can always handle the data stream coming from the S-LINK.

In the duplex version, a return channel exists which allows the LDC to pass information back to the LSC. The main function of this return channel is to transmit flow control commands from the ROMB to the FEMB. Thus a duplex S-LINK transmits only when the ROMB is available to read the data. When the ROMB is unavailable, data transfers from the FEMB to the S-LINK are inhibited. In addition, the return channel may be used to transmit signals on a set of return lines.

1.2 Data Sheet

This specification defines only the interface to the S-LINK. One consequence of this approach is that S-LINKs can be constructed using different physical media. Such S-LINKs may have different timing characteristics and data transfer rates. However, all S-LINKs will be accompanied by a Data Sheet which will detail these features. The user should therefore consult both this specification and the appropriate Data Sheet for the S-LINK which is to be used.

As an example, a dummy Data Sheet is available for consultation.

1.3 Implementation Guide

This specification is written from the point-of-view of the S-LINK user (that is, the designer of the FEMB or ROMB). For the designer of an S-LINK, an implementation guide is available which includes advice on how to implement the various features of the S-LINK.

2.0 Features of the S-LINK

2.1 Features common to simplex and duplex versions

1. **Control/Data bit:** All words transmitted are accompanied by an additional bit which enables the user to mark any word and thus identify the word with a private meaning (e.g. *block_address, event_header, end_of_block* etc.).
2. **Error Reporting:** An S-LINK detects transmission errors and reports these using the LDERR# line. In addition, the *data error* LED is illuminated and held until reset.
3. **Variable Data Width:** An S-LINK may be built with a data width of 8-bit, 16-bit or 32-bit or the width may be switchable with different widths having the same data transfer rate. The data width and possibility of switching will be defined in the S-LINK Data Sheet.
4. **Test Function:** The LSC and LDC can be switched to a test mode where the LSC transmits a fixed pattern which the LDC verifies. If any data errors are detected, the LDC illuminates the data error LED. The test pattern can be transferred to the ROMB by the LDC if desired.
5. **Reset Function:** A hard reset function is provided on both the LSC and the LDC.

2.2 Features found only with the duplex version

The duplex version allows the LDC to transmit information back to the LSC. This provides two additional features for the user;

1. **Flow Control:** The ROMB can assert a signal, UXOFF#, at the LDC which causes it to transmit an *XOFF* code to the LSC. This stops data transmission from the LSC. When the signal is de-asserted, an *XON* code is transmitted to the LSC which allows transmission to resume.
2. **Return Lines:** The state of four lines is continually sampled at the LDC, transmitted back to the LSC and presented to the FEMB. To the user, this looks like four wires running back from the LDC to the LSC.

2.3 Compatibility

A system of FEMB and ROMB which have been designed for use with a simplex S-LINK will function equally well with a duplex S-LINK.

If the FEMB and ROMB have been designed for a duplex S-LINK, the system will function with a simplex S-LINK in that data will be transmitted but the S-LINK will not handle flow control requests nor will the return lines function. Such a situation could lead to data loss.

This page intentionally left blank

3.0 Definitions

3.1 Hardware Components

An S-LINK is composed of two components: The *Link Source Card* (LSC) which is mounted on the user's front-end electronics (called the *Front-end Motherboard:* FEMB) and is the transmitter of data. The *Link Destination Card* (LDC) is mounted on the user's data collection electronics (called the *Read-out Motherboard:* ROMB) and is the receiver of data. When the LSC and LDC are referred to together, they are called the S-LINK.

3.2 Terminology

To avoid confusion, certain keywords have special meanings:

- *Shall* indicates a mandatory requirement. The instruction given has to be followed to conform to the specification. Failure to do so will lead to a non-conforming design which may not work.
- *Should* means that the designer does not need to follow the instruction given and can treat it as a recommendation.
- *May* means that an option is available.
- *Transfer* relates to data crossing the interface between the FEMB and the LSC or the interface between the LDC and the ROMB.
- *Transmit* relates to data travelling along the physical layer between the LSC and the LDC.

These keywords are only used in these contexts.

3.3 Signal Names

All signal names are printed in capital letters. Signals are defined as inputs or outputs to or from the S-LINK as follows:

- Signals which are generated by the user are prefixed with the letter "U", e.g. UD0, UWEN# etc. These signals are inputs to the S-LINK.
- Signals which are generated by the S-LINK are prefixed with the letter "L", e.g. LD0, LWEN# etc. These signals are outputs from the S-LINK.
- All signals which have an active state are **active when low** and **inactive when high**. Such signal names are terminated with a "**#**" character. *Low* and *High* refer to the signal levels which are defined electrically in Table 19 and Table 20.

Note that this convention applies in the same way at each end of the S-LINK, i.e. at the LSC and LDC.

3.4 Signal Line Functions

The signal lines for the LSC are described in Table 1. The signal lines for the LDC are described in Table 2.

TABLE 1. Signal Descriptions for the LSC

Pin Symbol	Pin Name	I/O	Description
UD[31..0]	User Data input lines	Input to S-LINK	Data on these lines is transferred to the LSC on a low-to-high transition of UCLK when UWEN is low. UD[3..0] are ignored if UCTRL# is low. Synchronous with UCLK.
LFF#	Link Full Flag	Output from S-LINK	Data *shall* only be written to the S-LINK when this line is high. After it goes low, up to two more words *may* be written. Functional when S-LINK is in test mode. Undefined when URESET# is low. Synchronous with UCLK.
URESET#	User Reset line	Input to S-LINK	When low initiates a reset cycle. Asynchronous.
UTEST#	User Test line	Input to S-LINK	When low switches the LSC to test mode. Causes LDOWN# to go low. Asynchronous.
UDW[1..0]	User Data Width lines	Input to S-LINK	Define the data width the S-LINK is to be operated in. Data width codes at LSC and LDC must be the same. Sampled after a reset cycle.
UCTRL#	User Control line	Input to S-LINK	When low indicates that the data to be transmitted is a control word. Causes UD[3..0] to be ignored. Synchronous with UCLK.
UWEN#	User Write Enable	Input to S-LINK	When low enables data to be transferred to the S-LINK on the low-to-high transition of UCLK. Synchronous with UCLK.
UCLK	User Clock	Input to S-LINK	Data is transferred to the S-LINK on the low-to-high transitions of UCLK when UWEN# is low. This is a free running clock.
LRL[3..0]	Link Return Lines	Output from S-LINK	These lines reflect the state of URL[3..0] at the LDC. In the simplex version these lines are not functional. A simplex FEMB *shall* leave these lines unconnected. A simplex LSC *shall* connect these lines to GND. Asynchronous, even relative to each other.
LDOWN#	Link Down	Output from S-LINK	When low indicates that the S-LINK is not operational. Asynchronous. Can go low due to: - S-LINK failure; then LDOWN# is latched low until cleared by a reset cycle. - S-LINK undergoing reset cycle, then LDOWN# goes high when reset cycle is complete. - S-LINK in test mode, then LDOWN# goes high when test mode is ended. The FEMB *shall* pull LDOWN# low if the LSC is not present or not powered up.

TABLE 2. Signal Descriptions for the LDC

Pin Symbol	Pin Name	I/O	Description
LD[31..0]	Link Data output lines	Output from S-LINK	Data present on these lines may be latched on the low-to-high transition of LCLK when LWEN# is low. LD[3..0] have special meanings when LCTRL# is low. Synchronous with LCLK.
UXOFF#	User Transmit Off	Input to S-LINK	When low, signals the LSC to stop transmitting data. Functions in test mode if UTDO# is low but does not stop transmission of test pattern if UTDO# is high. Asynchronous. In the simplex version this pin is not functional. A simplex ROMB *shall* pull-up this line to Vcc. A simplex LDC *shall* leave this line unconnected.
URESET#	User Reset line	Input to S-LINK	When low initiates a reset cycle. Asynchronous.
UTDO#	User Test Data Out	Input to S-LINK	When low, the received test pattern is transferred from the LDC to the ROMB during test mode. Sampled after a reset cycle.
UDW[1..0]	User Data Width lines	Input to S-LINK	Define the data width the S-LINK is to be operated in. Data width codes at LSC and LDC must be the same. Sampled after a reset cycle.
LCTRL#	Link Control line	Output from S-LINK	When low indicates that a control word is being transferred. Causes LD[3..0] to have a special meaning. Synchronous with LCLK.
LWEN#	Link Write Enable line	Output from S-LINK	When low indicates that valid data will be transferred to the ROMB on the low-to-high transition of LCLK. Synchronous to LCLK.
LCLK	Link Clock	Output from S-LINK	Data is transferred to the ROMB on each low-to-high transition of LCLK when LWEN# is low. This is a free-running clock if LDOWN# is high. If LDOWN# is low, this signal is undefined.
LDERR#	Link Data Error	Output from S-LINK	When low indicates that a data transmission error has occurred or that a pattern error has occurred during test mode. With word-by-word error reporting, LDERR# goes low with the word in error and with the control word for that block. With block basis error reporting, LDERR# goes low only with the control word for the block containing the word with error.
URL[3..0]	User Return Lines	Input to S-LINK	The state of these lines is sampled, transmitted back to the LSC and presented on LRL[3..0]. Asynchronous, even relative to each other. In the simplex version these pins are not functional. A simplex ROMB *shall* connect these lines to GND. A simplex LDC *shall* leave these lines unconnected.
LDOWN#	Link Down	Output from S-LINK	When low indicates that the S-LINK is not operational. Asynchronous. Can go low due to: - S-LINK failure; then LDOWN# is latched low until cleared by a reset cycle. - S-LINK undergoing reset cycle, then LDOWN# goes high when reset cycle is complete. - S-LINK in test mode, then LDOWN# goes high when test mode is ended. The ROMB *shall* pull LDOWN# low if the LDC is not present or not powered up.

This page intentionally left blank

4.0 S-LINK Usage Instructions

4.1 Overview

This Section describes in detail how the S-LINK can be used and how each feature works.

4.2 Maximum Clock Frequency and Data Transfer Rate

An S-LINK *shall* have a maximum clock frequency. This is defined as:

- 40 MHz

Note that the Data Transfer Rate depends on the physical implementation and the protocol used on the S-LINK. The Data Sheet which accompanies each S-LINK *shall* detail the Data Transfer Rate. The values of timing parameters are given in Table 3. Timing parameters which relate to the LSC are suffixed with a -S while those which relate to the LDC are suffixed with a -D.

TABLE 3. Timing Parameters

Symbol	Description	Min	Max	Units
t_{DS-S}, t_{DS-D}	Data Set-up time	10		ns
t_{DH-S}, t_{DH-D}	Data Hold time	1		ns
t_{ENS-S}, t_{ENS-D}	Enable Set-up time	10		ns
t_{ENH-S}, t_{ENH-D}	Enable Hold time	1		ns
t_{WFF-S}	Write Clock to Full Flag		12	ns
t_{CLK-S}, t_{CLK-D}	Clock Cycle time	25		ns
t_{CH-S}, t_{CH-D}	Clock High time	11		ns
t_{CL-S}, t_{CL-D}	Clock Low time	11		ns

4.3 Data Transmission

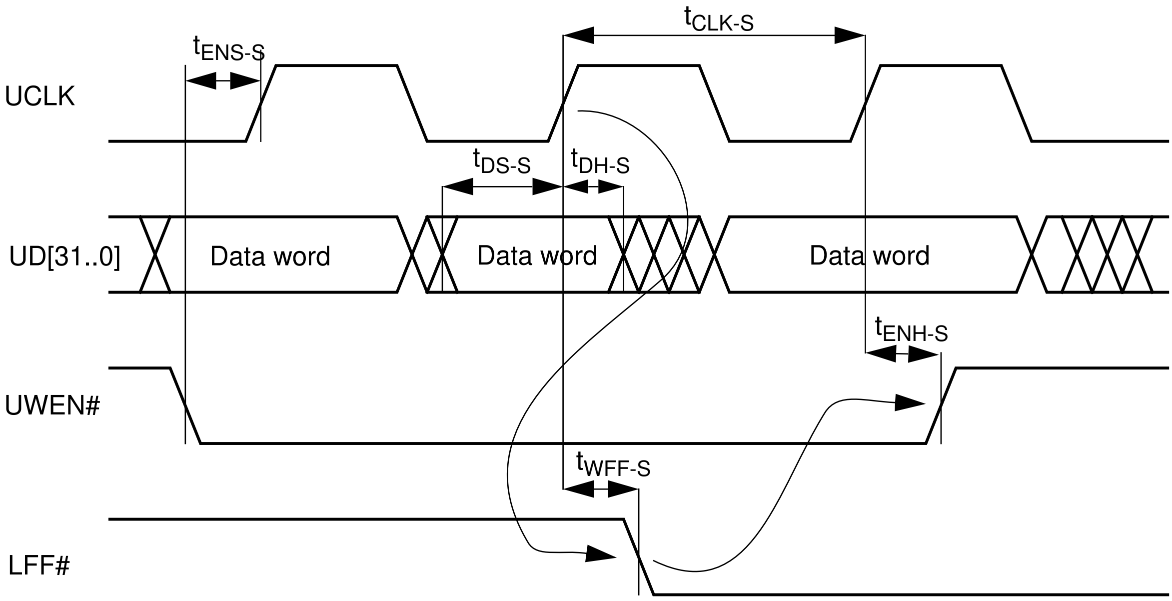
The S-LINK transmits data from the lines UD[31..0] and UCTRL# on the LSC to the lines LD[31..0] and LCTRL# on the LDC.

4.3.1 Data Transfer to the LSC

Data transfer to the LSC is based on writing to a FIFO memory. The user provides a free-running clock, UCLK, which *shall* be present at all times. When data is to be transferred to the LSC, the write-enable line, UWEN#, is set low and the data words are transferred on each subsequent low-to-high transition of UCLK.

Data can only be transferred to the LSC when Link Full Flag (LFF#) line is high. If this line goes low, the S-LINK will be able to receive up to two more data words (this is to allow the user time to react to LFF#). After transferring the extra words, the user *should not* try to transfer data to the S-LINK or data may be lost. A timing diagram is shown in Figure 2.

FIGURE 2. Data Transfer to the LSC



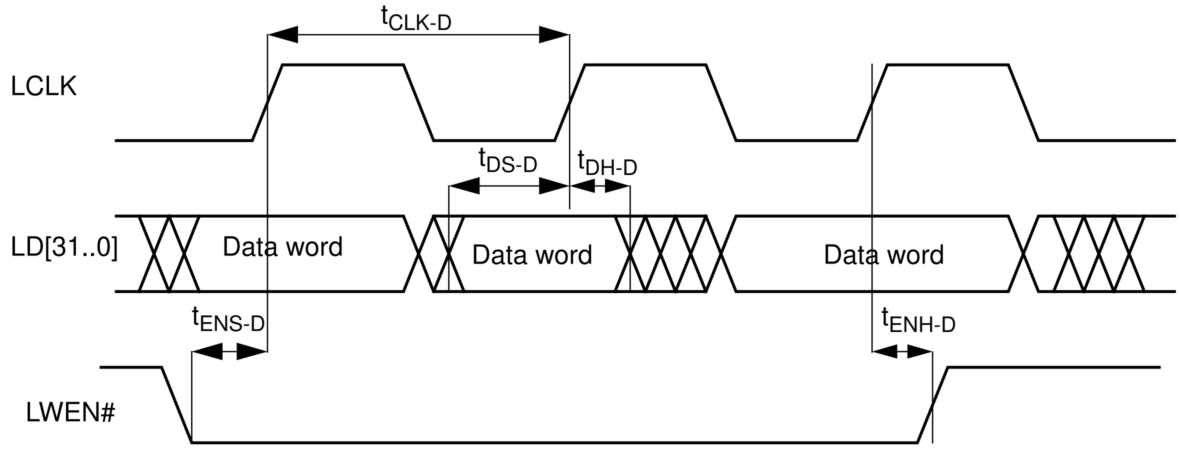
Note: In this diagram, only one extra data word is transferred after LFF# goes low. In fact, up to two words may be transferred.

4.3.2 Data Transfer from the LDC

Data is transferred out of the S-LINK as if the LDC were writing to a FIFO in the ROMB. The LDC provides a free-running clock (LCLK) which is always present if LDOWN# is high. If LDOWN# is low, LCLK is undefined.

When valid data arrives on the S-LINK, the LDC sets LWEN# low. The data words can then be latched on each low-to-high transition of LCLK. A timing diagram is shown in Figure 3.

FIGURE 3. Data Transfer from the LDC



4.4 Control/Data Bit

All words transmitted by the S-LINK are accompanied by a control/data bit which is carried on the lines UCTRL# and LCTRL#. This works in the following way: the line UCTRL# at the LSC, when low, indicates that the data lines UD[31..4] contain a user's private control code (e.g. *end_of_block, block_address* etc.). This causes the S-LINK to transmit this data in such a way that when the data is transferred from the LDC on lines LD[31..4], the line LCTRL# is set low for the duration of that word.

Note that when UCTRL# is set low, the data lines UD[3..0] and LD[3..0] are used by the S-LINK. That is, the data present on these lines at the LSC is ignored and the S-LINK itself generates the data which is transferred out of the LDC. Data lines UD[31..4] are transmitted and are transferred on LD[31..4] as normal. The reserved lines have the meanings detailed in Table 4. The reason for this scheme is to support the error detection function of the S-LINK which is described in Section 4.5.

For users who use the control/data bit to mark blocks of data, a data block is defined as the data words between two control words.

TABLE 4. Data Line Meanings When LCTRL# is Low

LD[31..4]	LD[3]	LD[2]	LD[1]	LD[0]
Same as UD[31..4]	Reserved for future use	Reserved for future use	**When 1:** Transmission error in Control Word. **When 0:** Control Word OK	**When 1:** Transmission error in previous data block **When 0:** Previous Data Block OK

This page intentionally left blank

4.5 Error Detection

The S-LINK provides an error check on data and control words but does not provide any error correction. Since different S-LINK implementations may use different error detection mechanisms, errors can be reported in one of two possible ways: on a block basis or on a word-by-word basis.

4.5.1 Block Basis Error Reporting

For S-LINKs which use cyclic redundancy checking for error detection, errors can only be reported after a block has been transmitted. Errors are therefore only reported with control words. If a block of data is transmitted and an error is detected by the S-LINK, it will set LDERR# low during the cycle containing the next control word. In addition, LD[1] is set low and LD[0] is set high for that word. The data error LED is illuminated and held.

An example of a data stream emerging from an S-LINK which uses block basis error reporting is shown in Table 5. In this example, the block length is four words. In the first block, there is no error. In the second block, an error occurs on the second data word. In the third block, an error occurs on the control word and in the fourth block an error occurs in both the second data word and in the control word.

TABLE 5. Block Basis Error Reporting (in this example the block length is 4 words).

LD[31..4]	LD[3..2]	LD[1]	LD[0]	LCTRL#	LDERR#
Data Word 1				1	1
Data Word 2				1	1
Data Word 3				1	1
Data Word 4				1	1
Control Word (EOB)	reserved	0	0	0	1
Data Word 1				1	1
Data Word 2 - with error				1	**1**
Data Word 3				1	1
Data Word 4				1	1
Control Word (EOB)	reserved	0	1	0	**0**
Data Word 1				1	1
Data Word 2				1	1
Data Word 3				1	1
Data Word 4				1	1
Control Word (EOB) - with error	reserved	1	0	0	**0**
Data Word 1				1	1
Data Word 2 - with error				1	**1**
Data Word 3				1	1
Data Word 4				1	1
Control Word (EOB) - with error	reserved	1	1	0	**0**

4.5.2 Word-by-Word Error Reporting

For S-LINKs which use parity checking for error detection, errors can also be reported on a word-by-word basis. If a transmission error is detected on a word, the line LDERR# is set low for one clock cycle during the transfer of the word containing the error. On the next control word transferred, LDERR# is again set low. In addition, LD[1] is set low and LD[0] is set high. If the word containing the error is a control word, LD[1] is set high and LD[0] is set high. The data error LED is illuminated and held.

An example of a data stream emerging from an S-LINK which uses word-by-word error reporting is shown in Table 6. In this example, the block length is four words. In the first block, there is no error. In the second block, an error occurs on the second word. In the third block, an error occurs on the control word and in the fourth block an error occurs in both the second data word and in the control word.

Thus, word-by-word error reporting is exactly the same as block basis error reporting with the addition of LDERR# being set low on the actual word with an error.

TABLE 6. Word-by-Word Error Reporting (in this example the block length is 4 words).

LD[31..4]	LD[3..2]	LD[1]	LD[0]	LCTRL#	LDERR#
Data Word 1				1	1
Data Word 2				1	1
Data Word 3				1	1
Data Word 4				1	1
Control Word (EOB)	reserved	0	0	0	1
Data Word 1				1	1
Data Word 2 - with error				1	**0**
Data Word 3				1	1
Data Word 4				1	1
Control Word (EOB)	reserved	0	1	0	**0**
Data Word 1				1	1
Data Word 2				1	1
Data Word 3				1	1
Data Word 4				1	1
Control Word (EOB) - with error	reserved	1	0	0	**0**
Data Word 1				1	1
Data Word 2 - with error				1	**0**
Data Word 3				1	1
Data Word 4				1	1
Control Word (EOB) - with error	reserved	1	1	0	**0**

This page intentionally left blank

4.6 Flow Control

This feature is available in the duplex version of the S-LINK only.

If the ROMB reaches a state in which it cannot process new data words coming from the LDC, it can stop the flow of data by setting the line UXOFF# low. This causes the LDC to send an *XOFF* command back to the LSC which forces it to stop transmitting data. If the LSC has a buffer memory the LSC may still receive transfers from the FEMB but eventually the buffer will fill and this will cause LFF# to be set low. This data is not lost but is simply stored until UXOFF# goes high and data transmission resumes.

The user should be aware that transfers from the LDC to the ROMB will not stop immediately when UXOFF# is set low. There is a latency which is the sum of the reaction time of the LDC (to transmit an *XOFF* code to the LSC), the transmission time of the *XOFF* code to the LSC, the reaction time of the LSC (to stop transmitting data), and the transmission time of the last data word from the LSC. This could be quite large, for example, in the case of an S-LINK which transfers data words on a 20 ns cycle over a 200 m link, more than 100 words could be transferred from the LDC to the ROMB after UXOFF# is set low. The user should calculate this latency for the implementation in use and ensure that when the ROMB asserts UXOFF#, it still has sufficient capacity to receive latent transfers.

Equation 1 shows how to calculate the ROMB buffer size required for any particular implementation. Note that if a ROMB designed for one implementation is used in another which has different parameters (such as a longer transmission length) the flow control mechanism may not work.

$$RBS = \left(\frac{LDC_{rt} + [L \times UFD \times 2] + LSC_{rt}}{DTR}\right) \qquad \textbf{(EQ 1)}$$

Where:

RBS = ROMB Buffer Size (words)

LDC_{rt} = LDC reaction time to send *XOFF* after UXOFF# goes low (ns).

LSC_{rt} = LSC reaction time to stop transmitting data after *XOFF* received (ns).

L = Length of S-LINK (m).

UFD = Unit Fibre Delay - time for light to travel 1m in fibre (approx. 6 ns/m).

DTR = Data Transfer Rate (words/ns).

Note that if a ROMB is to be constructed which is intended for a simplex S-LINK, UXOFF# *shall* be pulled-up to V_{cc}. In this way, the ROMB will still function with a duplex S-LINK.

An example timing diagram is shown in Figure 4. In this diagram, the sequence of events is as follows;

1. The transfer of word **m** from the LDC to the ROMB causes the ROMB to set UXOFF# low. This is done asynchronously.
2. The LDC transmits an *XOFF* command back to the LSC. This causes the LSC to stop transmitting data. During the time taken for the XOFF command to travel back to the LSC, the LSC to respond and the last data word to be transmitted to the LDC, **n** additional words are received at the LDC.
3. At the LSC, data transmission stops with word **m+n**. The buffer fills after **w** more words are transferred and so LFF# is set low. In this case, one more word is transferred by the FEMB, although up to two words may be transferred. This is word **m+n+w+1**.
4. The FEMB does not transfer any more data to the LSC (UWEN# high).
5. At the LDC, no more data is being transferred to the ROMB so it has time to clear its buffer or process the data. After some time, it is ready to receive data again. To re-start the dataflow, the ROMB sets UXOFF# high.
6. On seeing UXOFF# go high, the LDC transmits an *XON* command back to the LSC. This causes the LSC begin transmitting data again. Again there is a delay while the XON command travels to the LSC, the LSC responds and the data travels up to the LDC. Eventually, the data arrives and the LDC sets LWEN# low to transfer it to the ROMB.
7. At the LSC, the buffer is cleared and so LFF# is set high.
8. The FEMB now can resume the transfer of data to the LSC and so sets UWEN# low. The re-established dataflow then continues until the end of data or a new *XOFF* state arises.

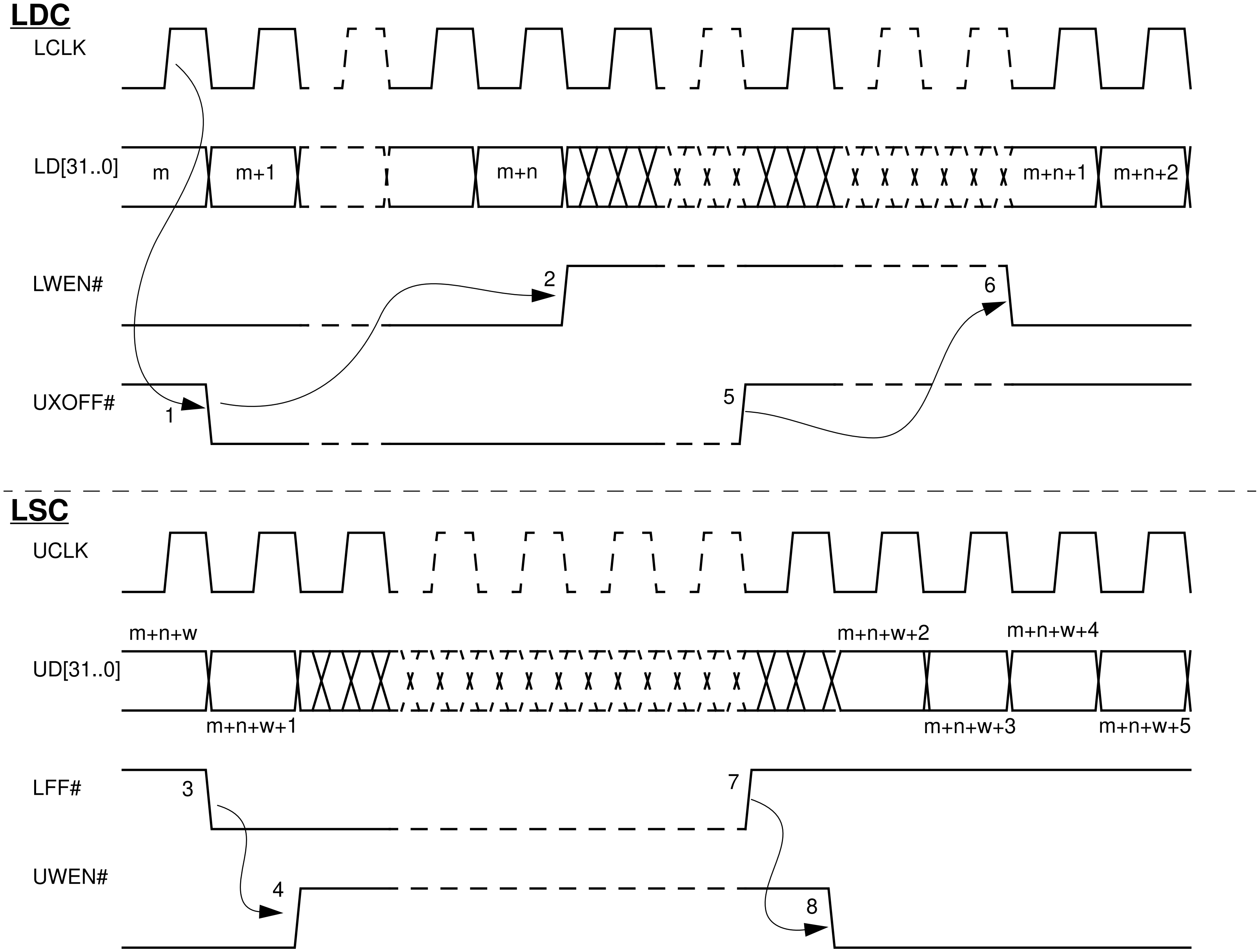


FIGURE 4. Flow Control: Sequence of Events

4.7 Return Lines

This feature is available in the duplex version of the S-LINK only.

Four lines are provided to allow the ROMB to send signals back to the FEMB. The lines URL[3..0] are inputs to the LDC. The LSC has output lines LRL[3..0] which reflect the state of URL[3..0]. The lines are updated frequently but there is no guaranteed delivery time nor is it guaranteed that the lines will be updated synchronously.

If a pulse is to be sent on these lines, the minimum pulse duration on URL[3..0] *shall* be 32 clock cycles of LCLK. The minimum pulse duration delivered on LRL[3..0] *shall* be 16 clock cycles of LCLK.

In this way, the lines have the appearance of four wires running back from the LDC to the LSC. They are intended for applying level-sensitive signals and slow control pulses to the FEMB and not for fast data transmission.

There is no equivalent of LDERR# on the return lines. Data words transmitted back to the LSC are checked for transmission errors but if an error is detected, the LSC simply does not update LRL[3..0]. If the error is a transient one, the lines will be updated on the next cycle. If the error is more serious and would prevent the minimum pulse of 16 clock cycles being transmitted, the LSC will set LDOWN# low.

The return lines continue to function during test mode (see Section 4.9). During a reset cycle (see Section 4.11), the return lines are set low and are updated as soon as possible after reset.

Note that if a FEMB or ROMB is to be constructed for a simplex S-LINK, these lines *shall* be connected to GND on the ROMB and left unconnected on the FEMB. In this way, the FEMB and ROMB will still work with a duplex S-LINK. In the case of a simplex S-LINK, the lines URL[3..0] on the LDC *shall* be left unconnected and the lines LRL[3..0] on the LSC *shall* be connected to GND.

4.8 Data Width Control

Various data widths are permitted for an S-LINK. It may also be possible to switch between different data widths which have the same data transfer rate. Permitted configurations are shown in Table 7.

Unused data lines *shall* be left unconnected on the LSC and connected to GND on the LDC.

If an S-LINK has a switchable data width, the data width to be used is selected by setting the lines UDW[1..0] according to Table 8. The Data Width lines are sampled after a reset cycle and the S-LINK configured then. Note that the same code must be selected at each end of the S-LINK. If the codes do not match, the S-LINK may function incorrectly. The data width configurations which an S-LINK can support *shall* be detailed in the S-LINK Data Sheet.

TABLE 7. Permitted Data Width Configurations

Data Width	Data lines used at LSC	Data lines used at LDC
32-bit only	UD[31..0]	LD[31..0]
16-bit only	UD[15..0]	LD[15..0]
8-bit only	UD[7..0]	LD[7..0]
32-bit or 16-bit	UD[31..0] UD[15..0]	LD[31..0] LD[15..0]
16-bit or 8-bit	UD[15..0] UD[7..0]	LD[15..0] LD[7..0]
32-bit, 16-bit or 8-bit	UD[31..0] UD[15..0] UD[7..0]	LD[31..0] LD[15..0] LD[7..0]

TABLE 8. Data Width Selection Codes

Data Width	UDW1	UDW0
32-bit	0	0
16-bit	0	1
8-bit	1	0
reserved	1	1

4.9 Test Function

A test mode is provided to exercise the physical link (such as fibre and connectors) and much of the S-LINK electronics. This test does not provide 100% fault coverage. If such a test is required the user should implement this using a test algorithm on the ROMB and FEMB.

The simplex and duplex versions of the S-LINK can be switched to test mode by holding the UTEST# signal low. This causes the LSC to illuminate a test-mode LED and to transmit a fixed pattern to the LDC. The pattern commences with all zeros transmitted on the data lines and with LCTRL# set low. It continues with a walking bit pattern where a single bit is transmitted first on bit 0, then on bit 1 and so on with each data line in succession. LCTRL# is set high. This is effectively a bit shift left on each successive word. The test pattern is shown in Table 9 (in the example shown, the data width is assumed to be 32-bit and so the cycle repeats after 33 words). If an S-LINK is in 8-bit or 16-bit data width, the cycle repeats after 9 or 17 words. At the LDC, a test-mode LED is illuminated and the LDC checks the incoming data stream. If any pattern or transmission errors are detected the data error LED on the LDC is illuminated.

TABLE 9. Test pattern (for an S-LINK in 32-bit data width)

Word	Hex value	Binary value	LCTRL#
0	0x0	00000000000000000000000000000000	0
1	0x1	00000000000000000000000000000001	1
2	0x2	00000000000000000000000000000010	1
3	0x4	00000000000000000000000000000100	1
4	0x8	00000000000000000000000000001000	1
5	0x10	00000000000000000000000000010000	1
---	---	---	1
29	0x10000000	00010000000000000000000000000000	1
30	0x20000000	00100000000000000000000000000000	1
31	0x40000000	01000000000000000000000000000000	1
32	0x80000000	10000000000000000000000000000000	1
---	---	cycle repeats until test mode is ended	---

A timing diagram for the signals at the LSC is shown in Figure 5 and their values are given in Table 10. UTEST# may be pulsed low, in which case one test pattern cycle will be transmitted, or it may be held low for as long as required in which case the test pattern will be transmitted continuously. When UTEST# is set high to end the test, the S-LINK will remain in test mode until the current test pattern has finished transmitting. The maximum time for this is implementation dependent.

FIGURE 5. Test mode at the LSC

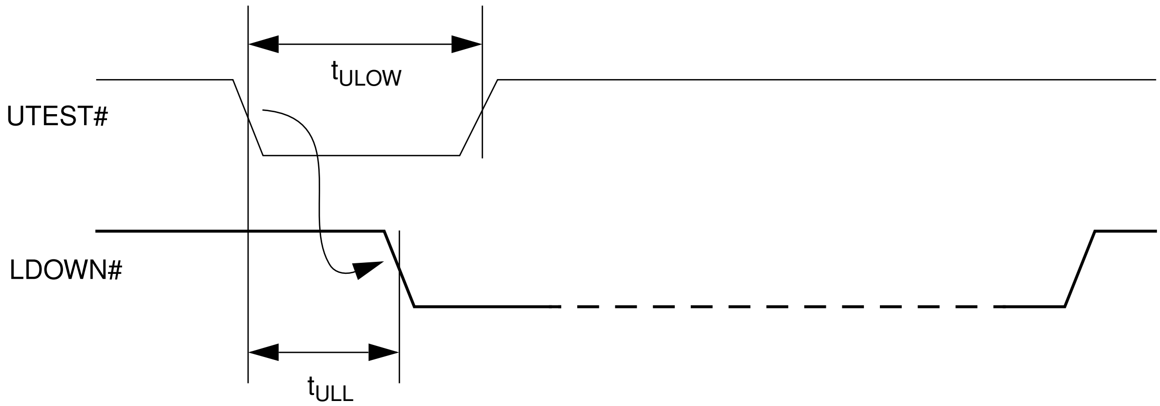


TABLE 10. Test Mode Timing Parameters

Symbol	Description	Min	Max	Unit
t_{ULL}	UTEST# low to LDOWN# low		4	Cycles of UCLK
t_{ULOW}	Minimum time for UTEST# low	4		Cycles of UCLK

Note that the default state is that the test data is **not** transferred to the ROMB (LWEN# is high). If desired, the ROMB can receive the test pattern by setting UTDO# low. When this is done, the test pattern is presented on the data lines, LD[31..0] and on LCTRL#. Any errors are reported as described in Section 4.5. A timing diagram is shown in Figure 6. In this diagram, LWEN# is shown to be constantly low so that a new word is transferred on each clock cycle. This is actually implementation dependent and LWEN# may be high on some clock cycles if new data words are not ready.

In a duplex S-LINK, UXOFF# functions in test mode. That is, if UTDO# is low and the test pattern is being transferred to the ROMB, setting UXOFF# low will cause the LSC to stop sending the test pattern. When UXOFF# goes high again, the test pattern transmission will resume. If UTDO# is high, UXOFF# has no effect on test pattern transmission. When test mode is ended, the LSC continues to transmit test words until the current cycle has completed.

Switching an S-LINK to test mode clears any error latches which may have been set during normal data transfer and clears any data which may be waiting for transmission. Similarly, when test mode is ended, any error latches set during test mode are cleared. This includes the data error LED. In addition, any data which might be in a buffer is cleared on leaving test mode. This is shown in Table 11.

TABLE 11. Clearing of error latches on entering and leaving test mode

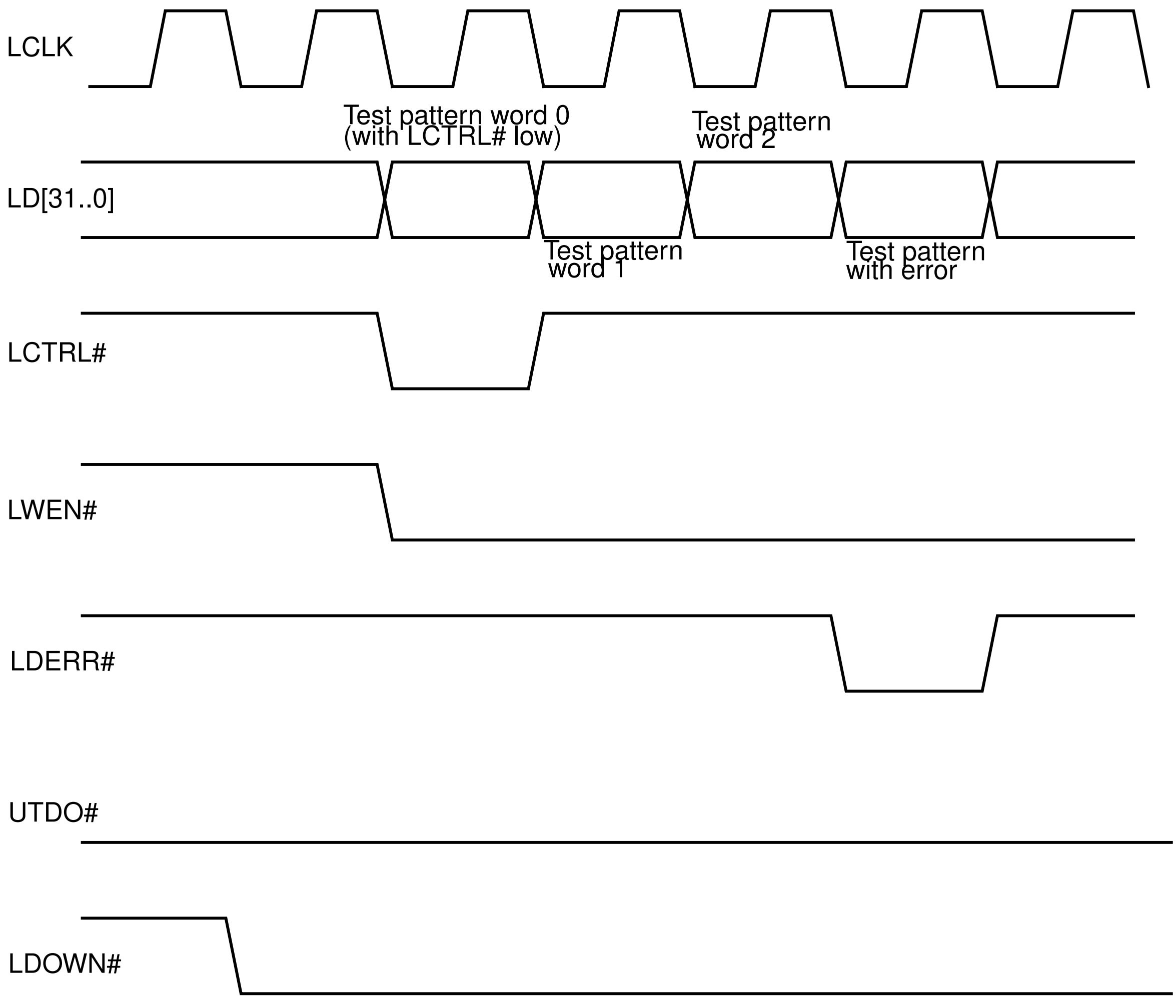
Data Transfer Mode
Switch to test mode - Clear errors here and clear any data buffers
Test Mode - block 1 Test Mode - block 2 ... Test Mode block N
Leave test mode - Clear errors here and clear any data buffers
Data Transfer Mode

From the user's point-of-view, the test mode has the same functionality in both the simplex and duplex versions of the S-LINK. However, in the duplex version the return physical link is also tested. An error in either physical link causes the data error LED on the LDC to be illuminated and latched.

Note that the return lines continue to function during test mode. That is, changes of state on lines URL[3..0] will be recognised and transmitted back to LRL[3..0] as described in Section 4.7.

LDOWN# is set low during test mode. This means that the FEMB shall not try to transfer data to the LSC during test mode.

FIGURE 6. Test mode at the LDC when UTDO# is set low



4.10 Link Down Function

A signal, LDOWN#, is provided on the LDC and LSC. If the LDC or LSC becomes aware of any problem which renders the S-LINK not functional, the LDC or LSC will set LDOWN# low and disable itself. If LDOWN# goes low during normal running, it is latched in that state even if the problem clears itself. LDOWN# can then only be removed by a reset cycle. This signal is asynchronous.

If either S-LINK card sets LDOWN# low, the other S-LINK card *should* set LDOWN# low, if this is possible.

LDOWN# is also set low during test mode. At the LSC, LDOWN# will go low when the LSC starts transmitting test patterns to the LDC. The time delay between UTEST# going low and LDOWN# going low is implementation dependent and is not specified. At the LDC, LDOWN# will go low at least one clock cycle of LCLK before the first test word is available. LDOWN# goes high again automatically when test mode is ended.

When a reset cycle is initiated at the LSC or LDC, LDOWN# goes low. When the reset cycle is complete, LDOWN# goes high automatically.

Notice that the only circumstance in which data can be transferred out of the LDC (LWEN# low, LCLK running) when LDOWN# is low is when the S-LINK is in test mode.

LDOWN# will also be low immediately on power-up, while the S-LINK card is completing its power-up configuration. When the power-up configuration is complete, LDOWN# will go high automatically.

The designer of the motherboard *shall* ensure that if the LSC or LDC is not powered-up or is not present, the motherboard will pull LDOWN# low.

4.11 Reset Function

An asynchronous reset is provided on the LSC and LDC on the line URESET#. At the LSC, when URESET# is set low, the LSC sets LDOWN# low to prevent data being transferred to the LSC. This happens within four clock cycles of UCLK. The LSC then initialises. When initialisation is complete, the LSC sets LDOWN# high. This is a signal to the FEMB that it can now remove the reset by setting URESET# high. After URESET# has been set high, the FEMB *shall* wait at least four clock cycles of UCLK before setting UWEN# low to transfer data to the LSC.

At the LDC, a similar procedure is followed: The ROMB sets URESET# low and the LDC responds by setting LDOWN# low and then initialising. When initialisation is complete, the LDC sets LDOWN# high.

If URESET# is set low on either S-LINK card, this *should* cause LDOWN# to be set low on the **other** S-LINK card. The other card will then have to be reset to clear LDOWN#.

This procedure is shown in Figure 7 and the values of the timing parameters are given in Table 12.

For a duplex S-LINK, the LSC and LDC can be reset in any order. For a simplex S-LINK, the LDC *shall* be reset first.

FIGURE 7. Reset procedure at the LSC and LDC

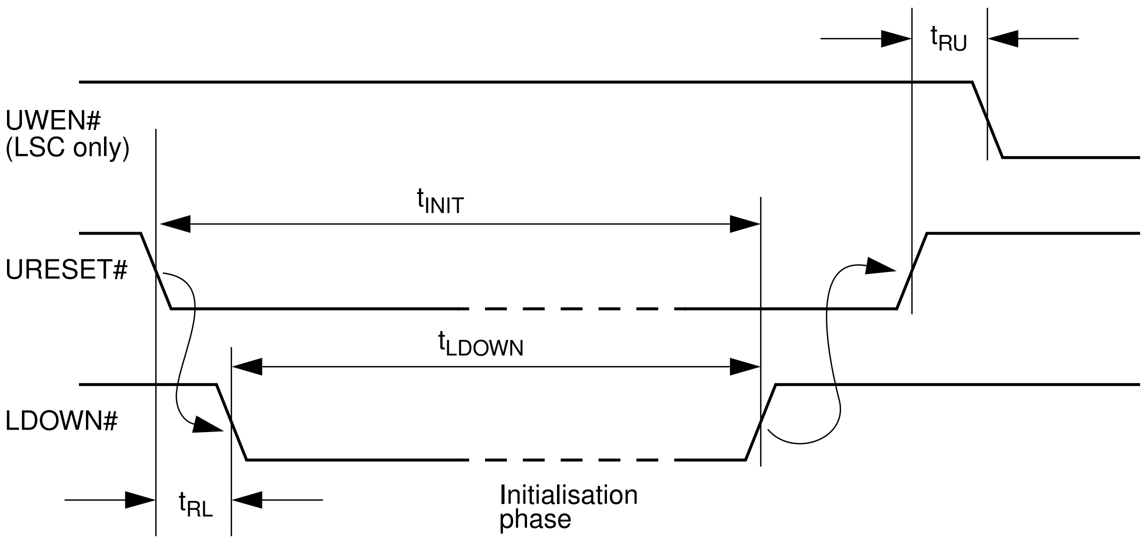


TABLE 12. Reset Cycle Timing Parameters

Symbol	Description	Min	Max	Units
t_{RL}	URESET# low to LDOWN# low		4	Cycles of UCLK or LCLK
t_{RU}	URESET# high to UWEN# low	4		Cycles of UCLK or LCLK
t_{INIT}	URESET# low to LDOWN# high		15	seconds
t_{LDOWN}	LDOWN# low duration	4		Cycles of UCLK or LCLK

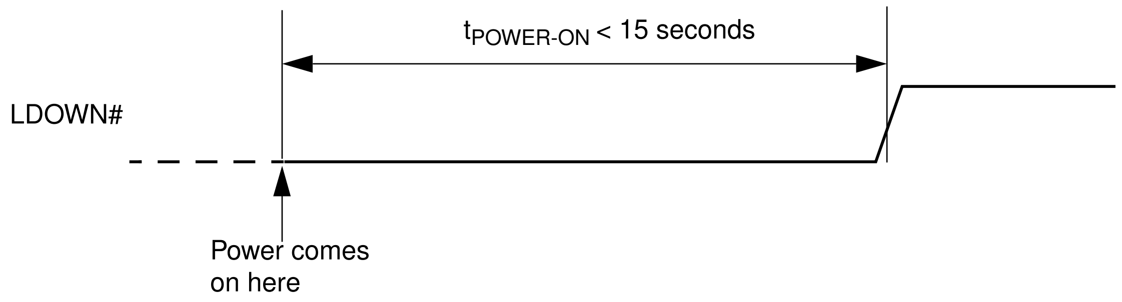
4.12 Power-on Sequence

On power-on, the S-LINK card will undergo a configuration routine which might take some time, especially if synchronisation is to be achieved over a long fibre link. During this time, LDOWN# will be held low. When the power-on sequence has been completed, LDOWN# will go high automatically.

The time taken for the power-on sequence is application dependent and may be quite large. Unless stated otherwise in the S-LINK Datasheet, $t_{POWER\text{-}ON}$ will be less than 15 seconds.

The power-on sequence is shown in Figure 8.

FIGURE 8. LDOWN# at Power-on



4.13 LED Indicators and Switch

A minimum set of LEDs is specified for the LSC and LDC. Various implementations of the S-LINK may have additional LEDs but all S-LINKs *shall* have at least this set. The LED functions are described in Table 13 and Table 14.

Note that when a data error is detected the data error LED is illuminated and held. To clear this state a momentary switch *shall* be provided.

All LEDs *shall* be visible from the front panel of the FEMB or ROMB.

TABLE 13. LEDs on the LSC

LED function	LED colour	Meaning when illuminated
Power indicator	Green	LSC is powered up
Test mode	Red	LSC is in test mode
Not LDOWN#	Green	LDOWN# is not low: there is no known problem with the S-LINK
LFF# active	Red	LFF# is active: no data can be transferred to the LSC

TABLE 14. LEDs on the LDC

LED function	LED colour	Meaning when illuminated
Power Indicator	Green	LDC is powered up
Test Mode	Red	LDC is in test mode
Data Error	Red	Data error has been detected
Not LDOWN#	Green	LDOWN# is not low: there is no known problem with the S-LINK
XOFF# active	Red	XOFF# is active: the ROMB has set XOFF# low thus signalling that it wants the transfer of data from the LDC to stop

4.14 Assignment of Unused Lines

It is intended that simplex and duplex S-LINKs and S-LINKs of different data width should be interchangeable as far as obvious limitations will allow. To ensure this, it is important that unused lines are assigned as defined in Table 15. Note that the assignments given in this table are also noted in the text.

TABLE 15. Assignment of Unused Lines

	on the motherboard		on the S-LINK	
Signal Lines	**Simplex**	**Duplex**	**Simplex**	**Duplex**
URL[3..0]	Connect to GND	Output	Not connected	Input
LRL[3..0]	Not connected	Input	Connect to GND	Output
UXOFF#	Pull up to Vcc	Output	Not connected	Input
UD[n..0]	Connect to GND	Connect to GND	Not connected	Not connected
LD[n..0]	Not connected	Not connected	Connect to GND	Connect to GND

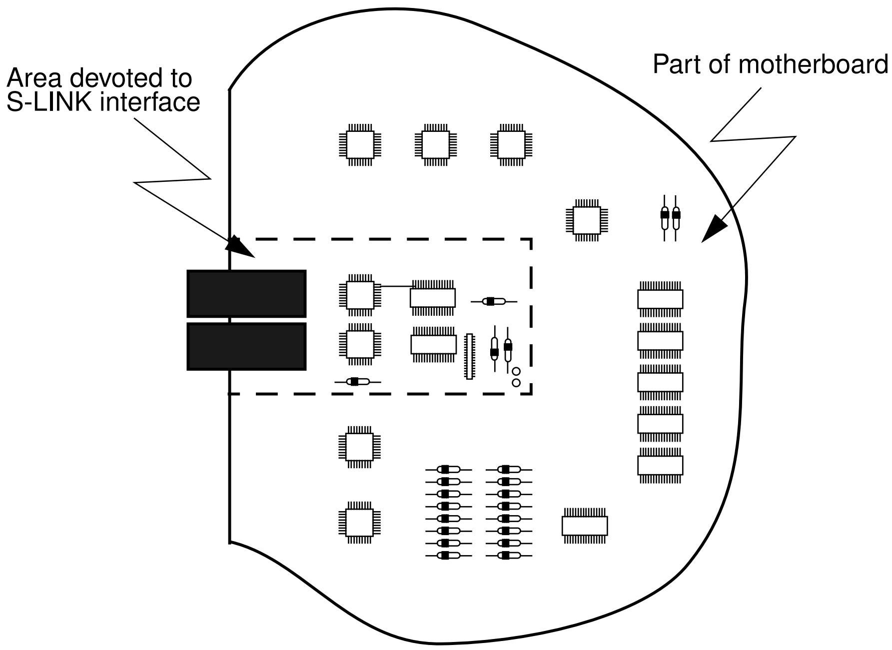
This page intentionally left blank

5.0 Physical Description

5.1 Example Implementations

This Specification is concerned with describing an *interface* between the user's motherboards and the S-LINK. The implementer of the S-LINK is free to use any physical arrangement desired. For example, one implementation could be to integrate the S-LINK interface into the motherboard as shown in Figure 9.

FIGURE 9. An S-LINK interface integrated into a motherboard



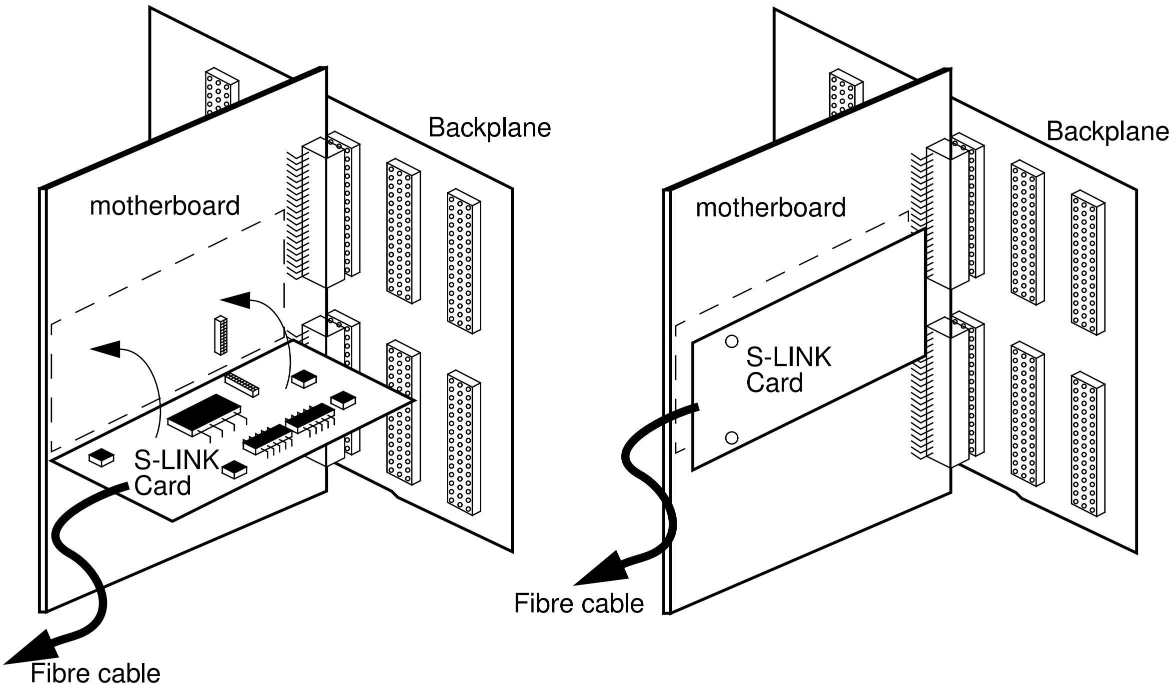
Alternatively, some users may wish to have separate S-LINK cards which are then mounted on the motherboard. If such users have no preferred physical arrangement, it is *recommended* that they construct the S-LINK cards according to the description given in Section 5.2.

An example of how such an implementation might appear is shown in Figure 10 which shows an S-LINK card mounted on a 6U VME motherboard.

5.2 Recommended Physical Arrangement

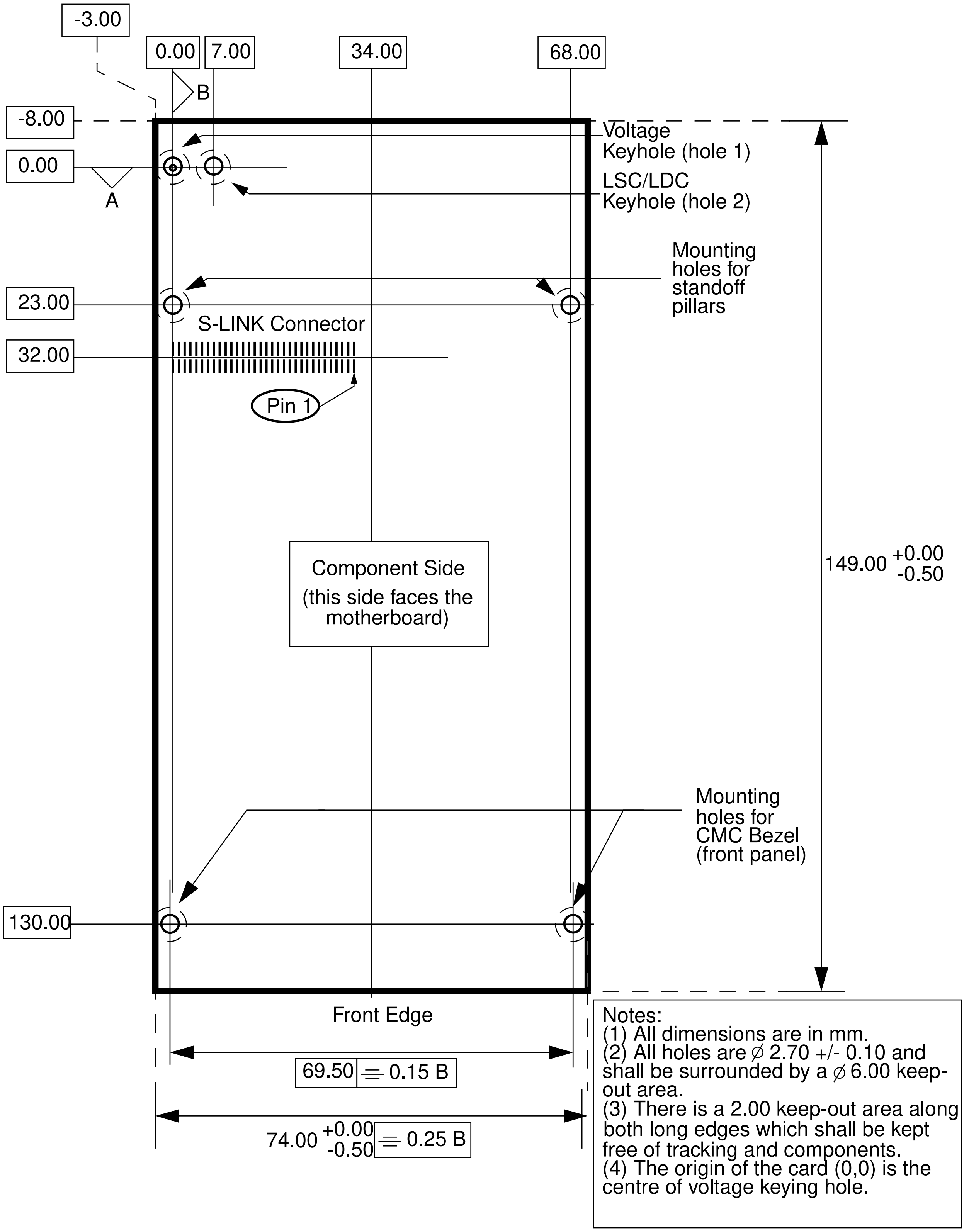
The S-LINK cards are based on single size Common Mezzanine Cards as defined in IEEE P1386/Draft 2.0 04-APR-1995, *Standard for a Common Mezzanine Card Family: CMC* (the CMC Standard).

FIGURE 10. A representation of how an S-LINK card is mounted on a 6U VME motherboard.



1. The physical shape of the S-LINK card *shall* be as defined in Figure 11.
2. Signal I/O and power distribution to the S-LINK card *shall* be handled by a single connector, positioned **outwith** the set of CMC Standard positions, as shown in Figure 11.

FIGURE 11. S-LINK card



3. The connector is a 64-pin surface-mount CMC connector and is a plug on both S-LINK cards (LSC and LDC) and a receptacle on both motherboards (FEMB and ROMB). Drawings of the surface mount pad layouts for the connectors are given in Figure 12 and Figure 13.

FIGURE 12. CMC “P” Plug Connector on S-LINK card with standoff drawing

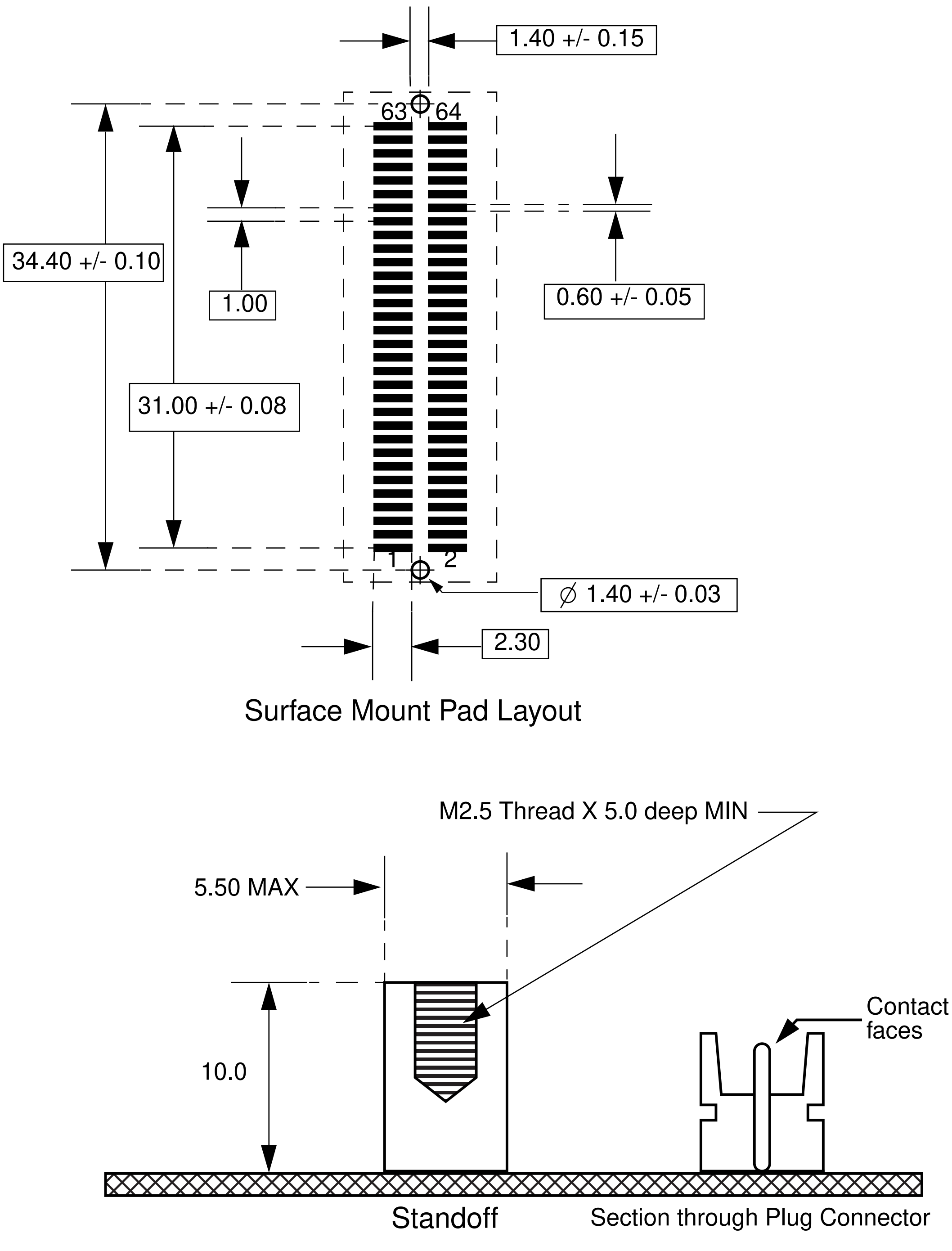
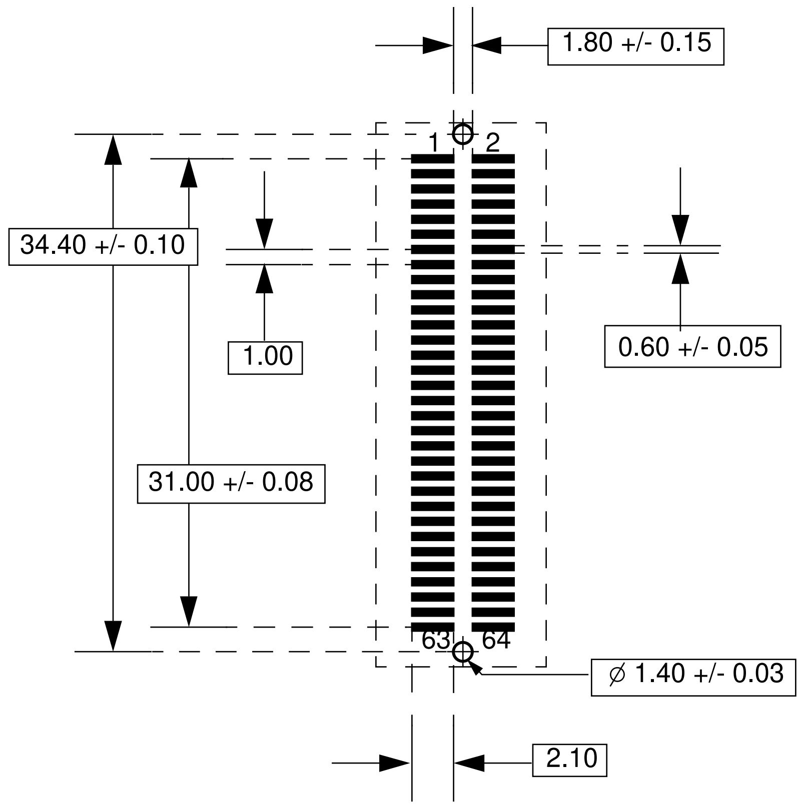
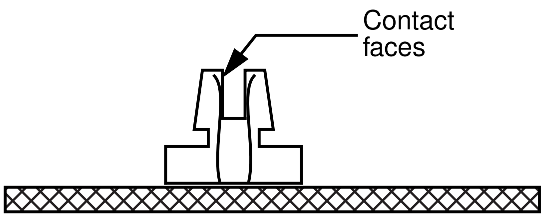


FIGURE 13. CMC "J" Receptacle Connector on motherboard



Surface Mount Pad Layout



Section through Receptacle Connector

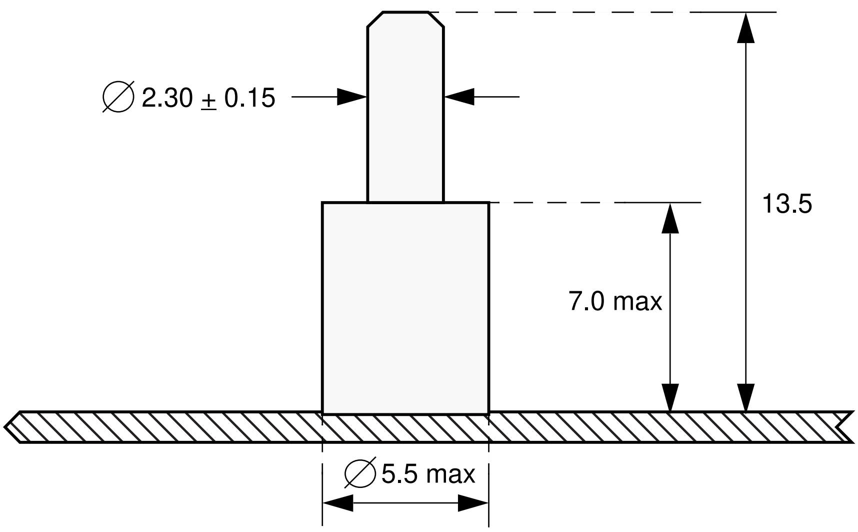
4. S-LINK cards may function with **either** a +5.0 V **or** with a +3.3 V supply. The LSC and LDC *shall* be provided with a keying hole which defines which voltage the card requires. The motherboard *shall* provide the keying pin.
5. S-LINK cards *shall* be provided with a keying hole which defines whether the card is a LSC or a LDC. The motherboard *shall* provide the keying pin.

   The arrangement of the keying pins is given in Table 16 and a technical drawing of a keying pin is given in Figure 14.

TABLE 16. Arrangement of Keying Pins

Type of card	Voltage Pins		LSC/LDC Pins	
	Has Pin 1	Has Hole 1	Has Pin 2	Has Hole 2
5V FEMB	yes		yes	
3.3V FEMB	no		yes	
5V LSC		yes		yes
3.3V LSC		no		yes
5V ROMB	yes		no	
3.3V ROMB	no		no	
5V LDC		yes		no
3.3V LDC		no		no

FIGURE 14. Keying Pin



6. The standoff pillars and the CMC bezel front panel are mounted on the S-LINK cards. The keying pins are mounted on the motherboard. To avoid ground loops and antenna effects, the standoff pillars, attachment areas, keying pins, keying holes and CMC bezel front-panel (if fitted) are to be grounded or isolated as described in Table 17 and Table 18.

The general rule is that each component is grounded with respect to the card on which it is mounted. Corresponding holes on the other card are then isolated. The only exception is the CMC bezel front panel which is completely isolated.

A drawing of a standoff pillar is given in Figure 12.

TABLE 17. Grounding considerations for FEMBs or ROMBs

Standoff attachment area (screw hole)	isolate
Keying pin	ground

TABLE 18. Grounding considerations for LSCs or LDCs

Standoff pillar	ground
Keying hole	isolate
CMC bezel front-panel (if fitted)	isolate

5.3 Component Height

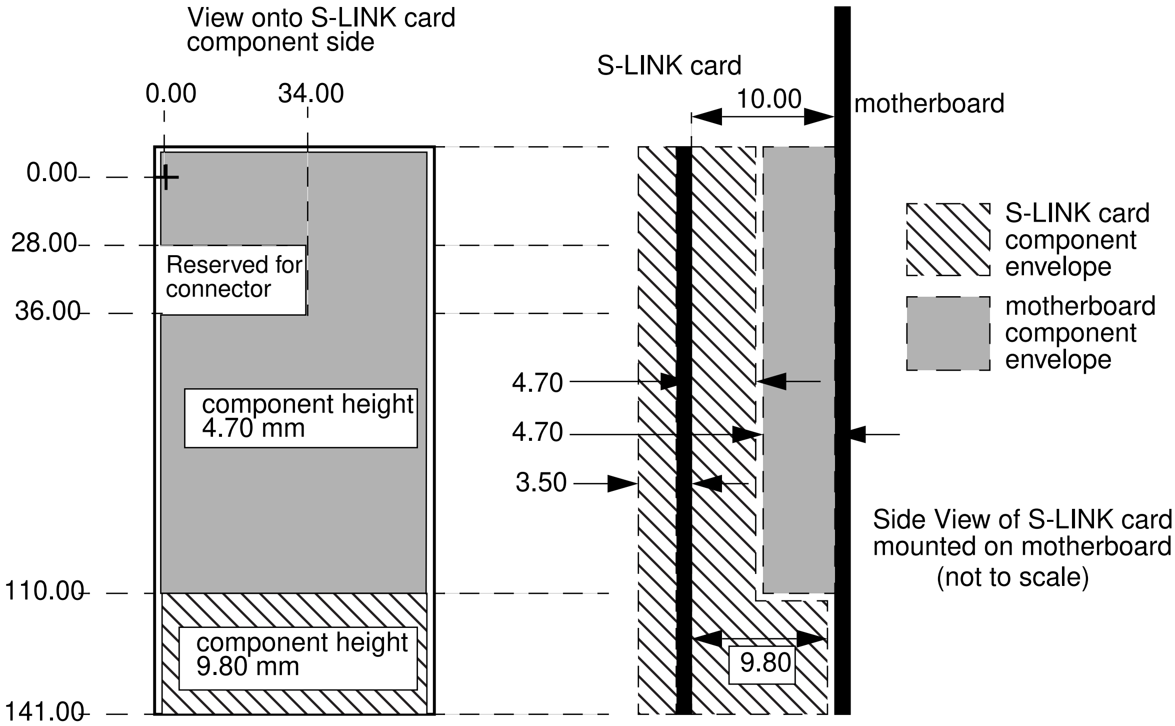
When fully mated, the CMC connectors leave a gap of 10.00 mm between the S-LINK card component side and the motherboard component side (the two cards mate with the component sides facing). This gap is shared between the two cards in the following way:

1. Up to 110.00, the component height can be 4.70 mm on both the S-LINK card and the motherboard. This leaves a clearance gap of 0.60 mm between component envelopes. Be careful not to foul the S-LINK connector and check that the components do not foul any PMC connectors which may be present on the motherboard.
2. At 110.00 and up to the edge of the card, the entire volume available is given to the S-LINK card. The component height on the S-LINK card can be 9.80 mm. No components are allowed on the motherboard in this region.

Components are permitted on the solder side of the S-LINK card provided that the component height plus card thickness does not exceed 3.50 mm.

This arrangement is shown in Figure 15.

FIGURE 15. Component heights on the S-LINK card



5.4 Front Panel

If the motherboard is fitted with a front panel it *shall* contain a CMC standard cut-out as detailed in Figure 16.

The S-LINK card *may* be fitted with a corresponding CMC bezel front-panel to form an EMC seal. The CMC bezel front-panel is detailed in Figure 17.

FIGURE 16. CMC standard cut-out for motherboard front-panels

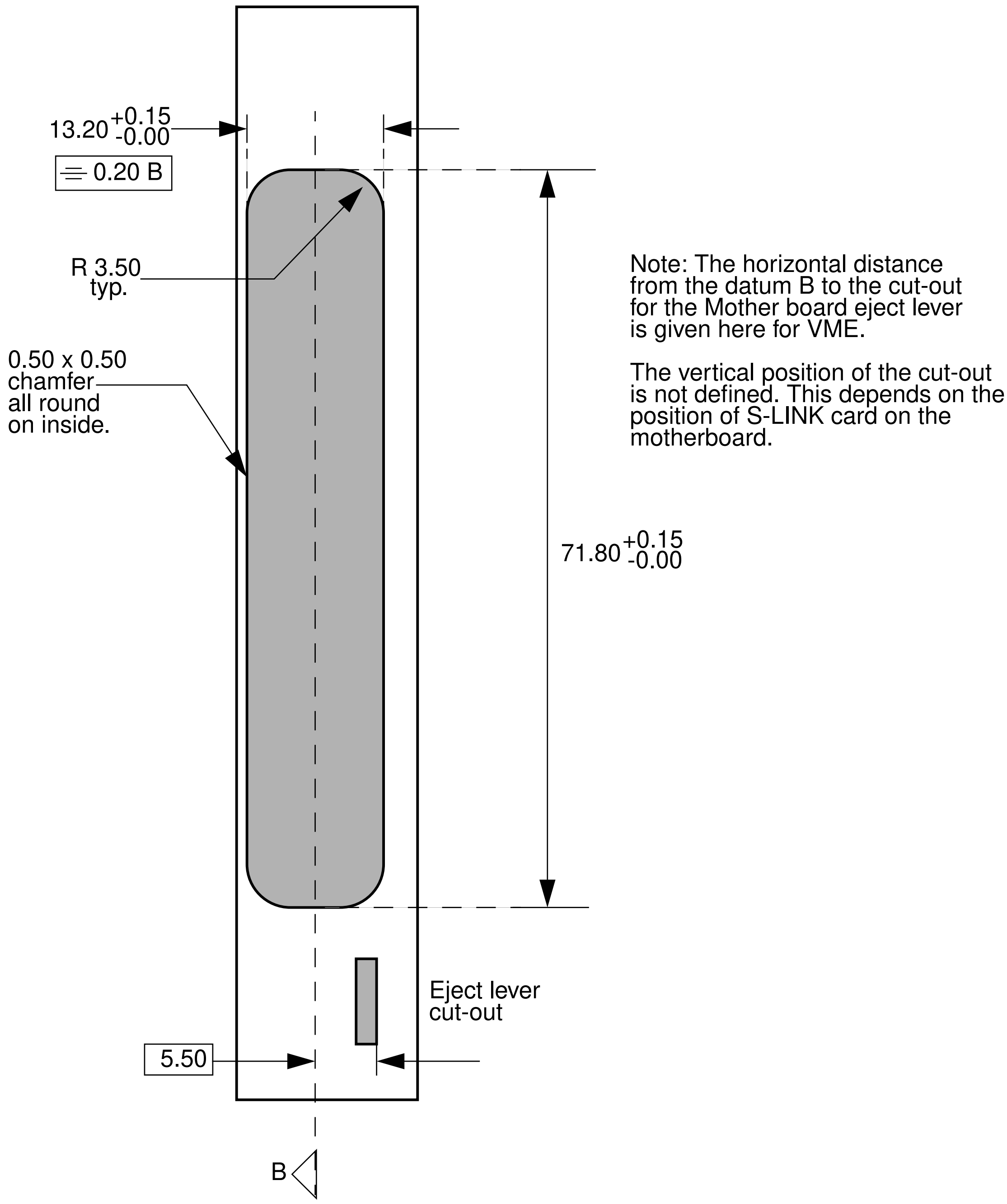
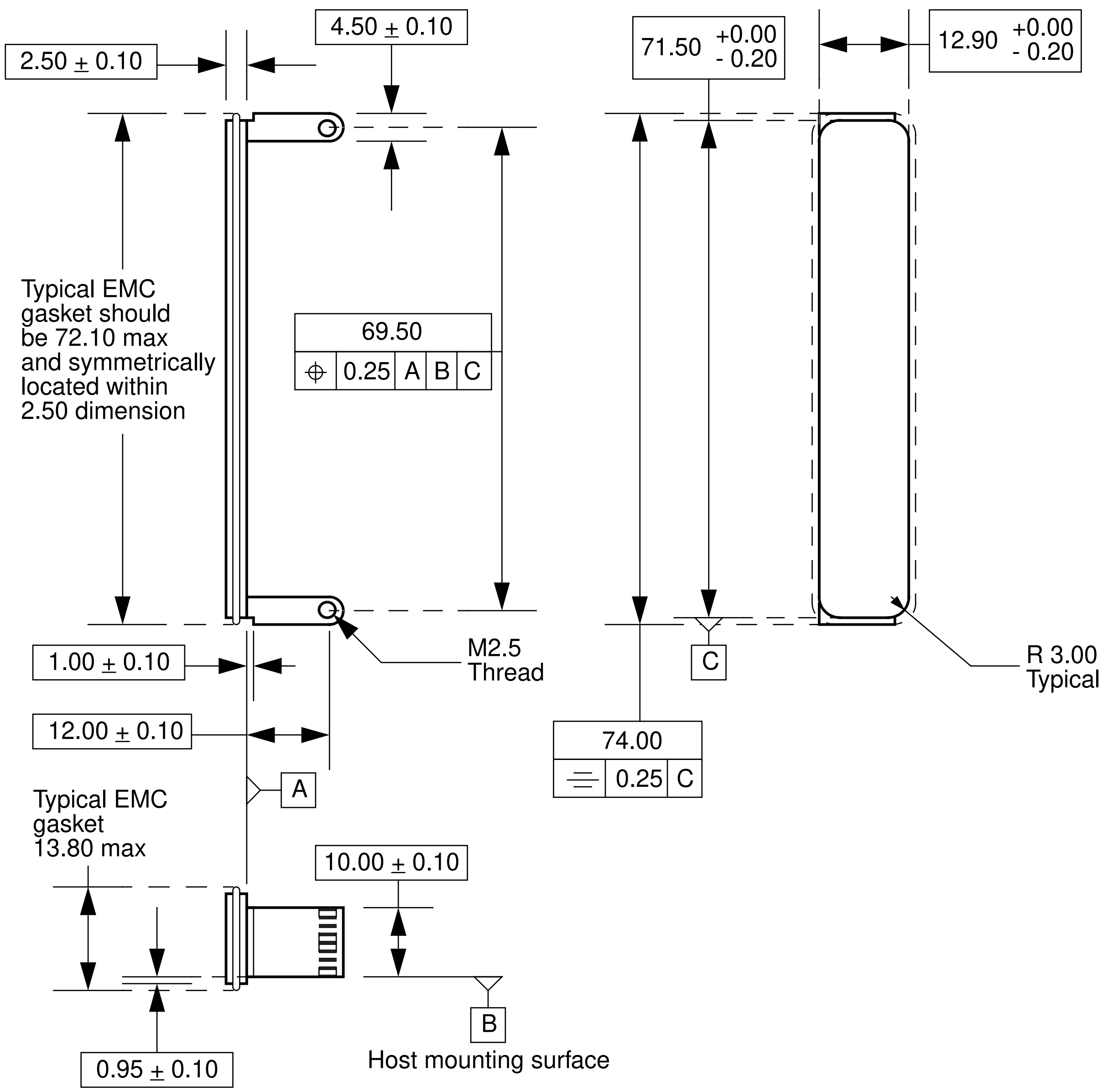


FIGURE 17. CMC bezel front panel (may be fitted to S-LINK cards if required)



6.0 Electrical Description

6.1 Power Requirements

The S-LINK cards *shall* operate from a single positive supply (V_{cc}) which *shall* be sourced directly from the motherboard. V_{cc} may be **either** +5.0 V **or** +3.3 V. In either case, the maximum power consumption *shall* be 7.5 W.

The designer *shall* define on the Data Sheet the supply voltage required and the maximum power consumption.

6.2 Signal Levels

The signal levels depend on the value of V_{cc}. The signal levels when V_{cc}= +5.0 V are shown in Table 19. The signal levels when V_{cc}= +3.3 V are shown in Table 20.

TABLE 19. DC Specifications for +5.0 V Signalling

Symbol	Description	Min	Max	Units
V_{CC}	Supply Voltage	4.75	5.25	Volts
V_{IH}	Input high voltage level	2.0	V_{CC} + 0.5	Volts
V_{IL}	Input low voltage level	-0.5	0.8	Volts
V_{OH}	Output high voltage level	2.4 (I_{OL} = -2mA)		Volts
V_{OL}	Output low voltage level		0.55 (I_{OL} = 3mA)	Volts

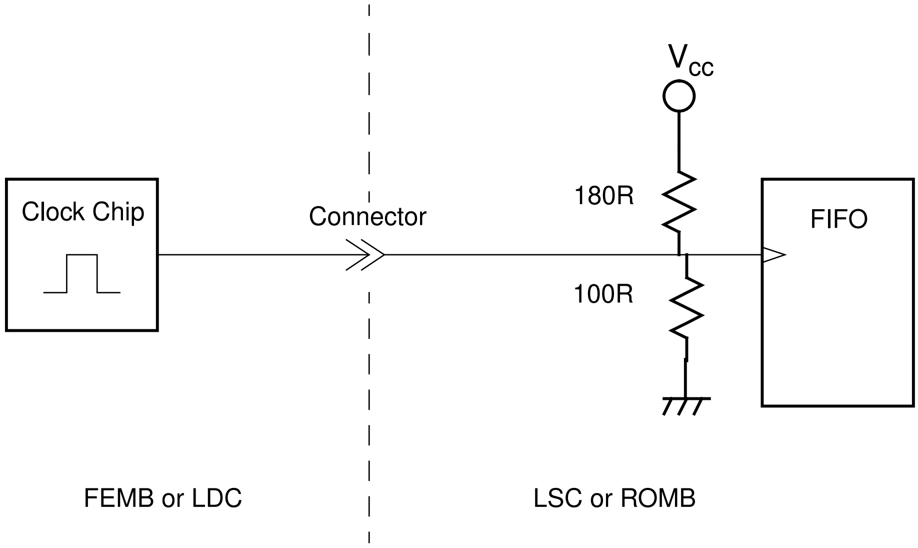
TABLE 20. DC Specifications for +3.3 V Signalling

Symbol	Description	Min	Max	Units
V_{CC}	Supply Voltage	3.0	3.6	Volts
V_{IH}	Input high voltage level	$0.5V_{CC}$	V_{CC} + 0.5	Volts
V_{IL}	Input low voltage level	-0.5	$0.3V_{CC}$	Volts
V_{OH}	Output high voltage level	$0.9V_{CC}$ (I_{OL} = -500 μA)		Volts
V_{OL}	Output low voltage level		$0.1V_{CC}$ (I_{OL} = 1500 μA)	Volts

6.3 Clock Signal Terminations

To ensure a clean clock signal, the designer of an LSC or a ROMB *should* terminate the incoming clock signals (UCLK and LCLK) from the FEMB and LDC respectively. An example of a termination resistance network which *may* be used is shown in Figure 18

FIGURE 18. Example of a clock signal termination resistance network



7.0 Pinout Diagrams

The pinout diagram for the LSC is shown in Table 21. The pinout diagram for the LDC is shown in Table 22. Both these diagrams represent the actual footprint of the connector when viewed **onto the motherboard**.

TABLE 21. Pinout Diagram for the LSC (view onto the motherboard)

1	LRL3	LRL2	2
3	Vcc	LRL1	4
5	Vcc	LRL0	6
7	LDOWN#	GND	8
9	GND	LFF#	10
11	UCLK	GND	12
13	GND	UWEN#	14
15	URESET#	GND	16
17	UDW1	UTEST#	18
19	UCTRL#	UDW0	20
21	UD31	Vcc	22
23	GND	UD30	24
25	UD29	UD28	26
27	UD27	GND	28
29	UD26	UD25	30
31	GND	UD24	32
33	UD23	UD22	34
35	UD21	GND	36
37	UD20	UD19	38
39	Vcc	UD18	40
41	UD17	UD16	42
43	UD15	GND	44
45	UD14	UD13	46
47	GND	UD12	48
49	UD11	UD10	50
51	UD9	Vcc	52
53	UD8	UD7	54
55	GND	UD6	56
57	UD5	UD4	58
59	UD3	GND	60
61	UD2	UD1	62
63	Vcc	UD0	64

TABLE 22. Pinout Diagram for the LDC (view onto the motherboard)

1	URL3	URL2	2
3	Vcc	URL1	4
5	LDERR#	URL0	6
7	LDOWN#	GND	8
9	GND	UXOFF#	10
11	LCLK	GND	12
13	GND	LWEN#	14
15	URESET#	GND	16
17	UDW1	UTDO#	18
19	LCTRL#	UDW0	20
21	LD31	Vcc	22
23	GND	LD30	24
25	LD29	LD28	26
27	LD27	GND	28
29	LD26	LD25	30
31	GND	LD24	32
33	LD23	LD22	34
35	LD21	GND	36
37	LD20	LD19	38
39	Vcc	LD18	40
41	LD17	LD16	42
43	LD15	GND	44
45	LD14	LD13	46
47	GND	LD12	48
49	LD11	LD10	50
51	LD9	Vcc	52
53	LD8	LD7	54
55	GND	LD6	56
57	LD5	LD4	58
59	LD3	GND	60
61	LD2	LD1	62
63	Vcc	LD0	64

8.0 S-LINK Type Naming Convention

To identify the features present on motherboards and S-LINK cards all such cards *shall* carry an S-LINK type on the silk-screen. It is recommended that this S-LINK type be close to the S-LINK connector position and that it be visible from the component side of the motherboard when the S-LINK card is mounted on the motherboard.

The S-LINK type is composed of a series of numbers and letters delimited by a dash (-). The required information is as follows;

1. Card Type: This is FEMB, LSC, LDC or ROMB.
2. Type of S-LINK: Simplex (S) or Duplex (D).
3. Maximum Clock Frequency in MHz: 40.
4. Error Detection Method: Block (B), Word-by-Word (W) or Don’t Care (X)[1].
5. Supply Voltage in Volts: 5.0 or 3.3.
6. Data Rate in Mbytes/sec (any integer).

As an example, an S-LINK Source Card for a Duplex S-LINK which can run at up to 40 MHz, using Block Basis error detection, a 5.0 V power supply and having a data transfer rate of 180 MBytes/sec would bear the S-LINK type;

LSC-D-40-B-5.0-180

1. Note that only a FEMB is “don’t care” regarding error detection method since the FEMB has nothing to do with error checking.

This page intentionally left blank

9.0 Finding and Printing this Document

This Specification is maintained on World Wide Web. The most up-to-date version can always be found on:

http://www.cern.ch/HSI/s-link/

If you have a hard-copy of this Specification, please check that the date on the front-page (top-left corner) matches the one in the WWW version.

If you are browsing this Specification on WWW and want a hard-copy you can either preview the PostScript Version and print it out using your local PostScript Viewer or you can use anonymous FTP to the machine www.cern.ch and then get the file:

/pub/hsi/s-link/s-link.ps

This page intentionally left blank

10.0 Copyright Statement

This page intentionally left blank

11.0 Revision History

- **12th September 1995**

  First version released.

- **20th September 1995**

  Name changed from *Standard Detector Link* to *S-LINK.*

  Flow control diagram edited to show resumption of dataflow.

  Keying pins position and function altered.

  Keying pin technical drawing and arrangement table added.

  Physical Description made a recommendation (was mandatory).

  S-LINK connector position moved to adjacent P13 (was adjacent P11).

  $\overline{\text{UNTD}}$ line changed to $\overline{\text{UTDO}}$

  $\overline{\text{LDOWN}}$ line added to LDC and pinout altered.

- **26th September 1995**

  Flow control description altered to take account of buffer in LSC.

  $\overline{\text{LDOWN}}$ line added to LSC and pinout altered.

  Link established LED changed to *not* $\overline{\text{LDOWN}}$.

  Output drive currents changed to follow those in PCI Specification.

  PCI connector positions removed from Technical Drawing.

- **2nd October 1995**

  Return lines made to function in test mode.

  World-Wide Web pages rearranged.

- **12th October 1995**

  Signals names made to look like those in PCI Specification e.g $\overline{\text{LDERR}}$ changed to LDERR# and UD31-0 changed to UD[31..0].

- **25th October 1995**

  Reset procedure re-defined to include LDOWN#.

  Three permissible clock rates defined and timing parameter values added.

  Error Detection function altered to allow two possibilities: on a word-by-word basis or on a block basis.

- **13th November 1995**

  References to actual Data Transfer Rate removed. This is implementation dependent.

  Duty cycle of UCLK and LCLK added.

  Section describing control/data bit expanded and tables added.

  LDERR# goes low on control word if there is an error in the previous block even in word-by-word error reporting.

  During test mode, data may still be transferred to the LSC (dependent on LFF#).

  URESET# is asynchronous. Also, timing diagram expanded.

- **5th December 1995**

  Technical drawings of CMC connectors added.

  Naming convention for LSCs, LDCs, FEMBs and ROMBs established.

  LDOWN# is latched when set by failure. Needs reset cycle to clear.

  LRL[3..0] are set low after reset cycle.

  UXOFF# defined as an asynchronous signal.

- **12th December 1995**

  Signal description tables expanded and made more comprehensive.

  UXOFF# functions during test mode if UTDO# is low but is inactive in test mode if UTDO# is high.

  LDOWN# low due to failure also disables S-LINK.

- **25th January 1996**

  Minor typographical corrections.

- **13th February 1996**

  Correction made to screw-hole spacing in Figure 11.

  LEDs added for XOFF# on the LDC and LFF# on the LSC

  Front Panel defined for motherboards.

  Paragraph on component height re-written (Section 5.3).

- **25th March 1996**

  Data carrying channel defined as the *forward channel.*

  ROMB buffer size equation added.

  Test mode clears errors on start of test and end of test.

  Power-up sequence defined in new sub-section.

  Keying pins and holes moved in Figure 11.

  Grounding considerations added for standoffs and keying pins.

  Technical drawing of CMC bezel front-panel added.

  UD25 and UD26 swapped on LSC pinout.

- **15th April 1996**

  t_{LDOWN} defined in Figure 7 and Table 12.

  Data buffers cleared on leaving test mode. Also mentioned that the FEMB should not try to transfer data to the LSC during test mode.

- **3rd May 1996**

  Copyright statement added

  Timing diagram for test mode at the LSC added (Figure 5).

- **29th May 1996**

  Data waiting for transmission is cleared on entering test mode.

- **27th March 1997**

  Recommendation on clock signal terminations added.

Made clear that LCLK is undefined if LDOWN# is low.

Reset at one end causes LDOWN# low at other and vice versa, if possible.

FEMB can transfer up to two words to LSC after LFF# goes low.

Maximum clock speed set at 40 MHz only.

This page intentionally left blank

12.0 Glossary

CMC	Common Mezzanine Card
FEMB	Front-End Motherboard
LCLK	Link Clock
LCTRL#	Link Control bit
LD[31..0]	Link Data
LDC	Link Destination Card
LDERR#	Link Data Error
LDOWN#	Link Down
LFF#	Link Full Flag
LRL[3..0]	Link Return Line
LSC	Link Source Card
LWEN#	Link Write Enable
ROMB	Read-Out Motherboard
UCLK	User Clock
UCTRL#	User Control bit
UD[31..0]	User Data
UDW	User Data Width
UTDO#	User Test Data Out
URESET#	User Reset
URL[3..0]	User Return Line
UTEST#	User Test
UWEN#	User Write Enable
UXOFF#	User Xmit Off

This page intentionally left blank